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REVISION HISTORY

1/11—Rev. 0 to Rev. A

Changes to Figure 1	1
Changes to Connecting and Using the AD8264-EVALZ Section and Figure 117	34
Changes to Figure 118	35

5/09—Revision 0: Initial Version

SPECIFICATIONS

$V_S = \pm 2.5$ V, $T_A = 25^\circ\text{C}$, $f = 10$ MHz, $C_L = 5$ pF, $R_L = 500 \Omega$ per output (VGAx, VOHx, VOLx), $V_{\text{GAIN}} = (V_{\text{GNHx}} - V_{\text{GNLO}}) = 0$ V, $V_{\text{VOCM}} = \text{GND}$, $V_{\text{OFSx}} = \text{GND}$, gain range = 6 dB to 30 dB, unless otherwise specified.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
GENERAL PERFORMANCE					
-3 dB Small Signal Bandwidth (VGAx)	$V_{\text{OUT}} = 10$ mV p-p		235		MHz
-3 dB Large Signal Bandwidth (VGAx)	$V_{\text{OUT}} = 1$ V p-p		150		MHz
-3 dB Small Signal Bandwidth (Differential Output) ¹	$V_{\text{OUT}} = 100$ mV p-p		80		MHz
-3 dB Large Signal Bandwidth (Differential Output) ¹	$V_{\text{OUT}} = 2$ V p-p		80		MHz
Slew Rate	VGAx, $V_{\text{OUT}} = 2$ V p-p		380		V/ μ s
	VGAx, $V_{\text{OUT}} = 1$ V p-p		290		V/ μ s
	Differential output, $V_{\text{OUT}} = 2$ V p-p		470		V/ μ s
	Differential output, $V_{\text{OUT}} = 1$ V p-p		220		V/ μ s
Input Bias Current	Pins IPPx	-8	-5	-3	μ A
Input Resistance	Pins IPPx at dc; $\Delta V_{\text{IN}}/\Delta I_{\text{BIAS}}$		4.2		M Ω
Input Capacitance	Pins IPPx		2		pF
Input Impedance	Pins IPPx at 10 MHz		7.9		k Ω
Input Voltage Noise			2.3		nV/ $\sqrt{\text{Hz}}$
Input Current Noise			2		pA/ $\sqrt{\text{Hz}}$
Noise Figure (Differential Output)	$V_{\text{GAIN}} = 0.7$ V, $R_S = 50 \Omega$, unterminated		9		dB
Output-Referred Noise (Differential Output)	$V_{\text{GAIN}} = 0.7$ V (Gain = 30 dB)		72		nV/ $\sqrt{\text{Hz}}$
	$V_{\text{GAIN}} = -0.7$ V (Gain = 6 dB)		45		nV/ $\sqrt{\text{Hz}}$
Output Impedance	VGAx, dc to 10 MHz		3.5		Ω
	Differential output, dc to 10 MHz		<1		Ω
Output Signal Range	Preamp		$ V_S - 1.3$		V
	VGAx, $R_L \geq 500 \Omega$		$ V_S - 1.3$		V
	Differential amplifier, $R_L \geq 500 \Omega$ per side		$ V_S - 0.5$		V
Output Offset Voltage	Preamp offset	-6	<1	+6	mV
	VGAx offset, $V_{\text{GAIN}} = 0.7$ V	-18	<5	+18	mV
	Differential output offset, $V_{\text{GAIN}} = 0.7$ V	-38	<10	+38	mV
DYNAMIC PERFORMANCE					
Harmonic Distortion	VGAx = 1 V p-p, differential output = 2 V p-p (measured at VGAx)				
HD2	$f = 1$ MHz		-73		dBc
HD3			-68		dBc
HD2	$f = 10$ MHz		-71		dBc
HD3			-61		dBc
HD2	$f = 35$ MHz		-60		dBc
HD3			-53		dBc
	VGAx = 1 V p-p, differential output = 2 V p-p (measured at differential output)				
HD2	$f = 1$ MHz		-78		dBc
HD3			-66		dBc
HD2	$f = 10$ MHz		-71		dBc
HD3			-43		dBc
HD2	$f = 35$ MHz		-56		dBc
HD3			-20		dBc
Input 1 dB Compression Point	$V_{\text{GAIN}} = -0.7$ V, $f = 10$ MHz		7		dBm ²
	$V_{\text{GAIN}} = +0.7$ V, $f = 10$ MHz		-9.6		dBm

AD8264

Parameter	Conditions	Min	Typ	Max	Unit
Two-Tone Intermodulation Distortion (IMD3)	$VGAx = 1 \text{ V p-p}, f_1 = 10 \text{ MHz}, f_2 = 11 \text{ MHz}$ $VGAx = 1 \text{ V p-p}, f_1 = 35 \text{ MHz}, f_2 = 36 \text{ MHz}$ $V_{OUT} = 2 \text{ V p-p}, f_1 = 10 \text{ MHz}, f_2 = 11 \text{ MHz}$ $V_{OUT} = 2 \text{ V p-p}, f_1 = 35 \text{ MHz}, f_2 = 36 \text{ MHz}$ $VGAx = 1 \text{ V p-p}, f = 10 \text{ MHz}$	-68			dBc
Output Third-Order Intercept		-51			dBc
		-49			dBc
		-34			dBc
		32			dBm
		19			dBV_{RMS}
	$VGAx = 1 \text{ V p-p}, f = 35 \text{ MHz}$	23			dBm
		10			dBV_{RMS}
	$V_{OUT} = 2 \text{ V p-p}, f = 10 \text{ MHz}$	30			dBm
		17			dBV_{RMS}
	$V_{OUT} = 2 \text{ V p-p}, f = 35 \text{ MHz}$	21			dBm
		8			dBV_{RMS}
Overload Recovery	$V_{GAIN} = 0.7 \text{ V}, V_{IN} \text{ stepped from } 0.1 \text{ V p-p to } 1 \text{ V p-p}$	25			ns
Group Delay Variation	$1 \text{ MHz} < f < 100 \text{ MHz}$, full gain range	± 1			ns
ACCURACY					
Absolute Gain Error ³	$-0.7 \text{ V} < V_{GAIN} < -0.6 \text{ V}$ $-0.6 \text{ V} < V_{GAIN} < -0.5 \text{ V}$ $-0.5 \text{ V} < V_{GAIN} < +0.5 \text{ V}$ $0.5 \text{ V} < V_{GAIN} < 0.6 \text{ V}$ $0.6 \text{ V} < V_{GAIN} < 0.7 \text{ V}$	0	0.2 to 2	3	dB
		-1.25	± 0.35	+1.25	dB
		-1	± 0.25	+1	dB
		-1.25	± 0.35	+1.25	dB
		-3	-0.2 to -2	0	dB
Gain Law Conformance ⁴	$-0.5 \text{ V} < V_{GAIN} < +0.5 \text{ V}, \pm 2.5 \text{ V} \leq V_s \leq \pm 5 \text{ V}$ $-0.5 \text{ V} < V_{GAIN} < +0.5 \text{ V}, -40^\circ\text{C} \leq T_A \leq +105^\circ\text{C}$		± 0.2		dB
			± 0.3		dB
Channel-to-Channel Matching	Single IC, $-0.5 \text{ V} < V_{GAIN} < +0.5 \text{ V}, -40^\circ\text{C} \leq T_A \leq +105^\circ\text{C}$ Multiple ICs, $-0.5 \text{ V} < V_{GAIN} < +0.5 \text{ V}, -40^\circ\text{C} \leq T_A \leq +105^\circ\text{C}$	-0.5	$\pm 0.1 \text{ to } \pm 0.25$	+0.5	dB
			± 0.25		dB
GAIN CONTROL INTERFACE					
Gain Scaling Factor	$-0.5 \text{ V} < V_{GAIN} < +0.5 \text{ V}$	19.5	20.0	20.5	dB/V
Over Temperature	$-40^\circ\text{C} \leq T_A \leq +105^\circ\text{C}$		20 ± 0.5		dB/V
Gain Range			24		dB
Gain Intercept to VGAx		11.5	11.9	12.2	dB
Over Temperature	$-40^\circ\text{C} \leq T_A \leq +105^\circ\text{C}$		11.9 ± 0.4		dB
Gain Intercept to Differential Output		17.5	17.9	18.2	dB
Over Temperature	$-40^\circ\text{C} \leq T_A \leq +105^\circ\text{C}$		17.9 ± 0.4		dB
GNHx Input Voltage Range	$GNLO = 0 \text{ V}$, no gain foldover	$-V_s$		$+V_s$	V
Input Resistance	$\Delta V_{IN}/\Delta I_{BIAS}, -0.7 \text{ V} < V_{GAIN} < +0.7 \text{ V}$		70		$\text{M}\Omega$
GNHx Input Bias Current	$-0.7 \text{ V} < V_{GAIN} < 0.7 \text{ V}$	-0.9	-0.4	0	μA
Over Temperature	$-0.7 \text{ V} < V_{GAIN} < 0.7 \text{ V}, -40^\circ\text{C} \leq T_A \leq +105^\circ\text{C}$		$-0.4 \pm +0.2$		μA
GNLO Input Bias Current	$-0.7 \text{ V} < V_{GAIN} < 0.7 \text{ V}$		-1.2		μA
Over Temperature	$-0.7 \text{ V} < V_{GAIN} < 0.7 \text{ V}, -40^\circ\text{C} \leq T_A \leq +105^\circ\text{C}$		$-1.2 \pm +0.4$		μA
Response Time	24 dB gain change		200		ns
OUTPUT BUFFER					
VOCM Input Bias Current		0.3	1.5	2.5	nA
Over Temperature	$-40^\circ\text{C} \leq T_A \leq +105^\circ\text{C}$		1.5 ± 0.3		nA
VOCM Input Voltage Range	$OFs_x = 0 \text{ V}, VGAx = 0 \text{ V}$	-1.4		+1.4	V
Gain (VGAx to Differential Output)		5.75	6	6.25	dB
Over Temperature	$-40^\circ\text{C} \leq T_A \leq +105^\circ\text{C}$		6 ± 0.5		dB

Parameter	Conditions	Min	Typ	Max	Unit
POWER SUPPLY					
Supply Voltage		±2.5		±5	V
Power Consumption					
Quiescent Current	$V_S = \pm 2.5 \text{ V}$	65	79	88	mA
	$V_S = \pm 2.5 \text{ V}, -40^\circ\text{C} \leq T_A \leq +105^\circ\text{C}$		79 ± 25		mA
	$V_S = \pm 3.3 \text{ V}$	70	85	95	mA
	$V_S = \pm 3.3 \text{ V}, -40^\circ\text{C} \leq T_A \leq +105^\circ\text{C}$		85 ± 30		mA
	$V_S = \pm 5 \text{ V}$	81	99	110	mA
	$V_S = \pm 5 \text{ V}, -40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}^5$		99 ± 30		mA
Power Dissipation	$V_S = \pm 2.5 \text{ V}$		395		mW
	$V_S = \pm 3.3 \text{ V}$		560		mW
	$V_S = \pm 5 \text{ V}$		990		mW
PSRR	From VPOS to differential output, $V_{\text{GAIN}} = 0.7 \text{ V}$		–15		dB
	From VNEG to differential output, $V_{\text{GAIN}} = 0.7 \text{ V}$		–15		dB

¹ Differential Output = (V_{OHx} – V_{OLx}).

² All dBm values are calculated with 50 Ω reference, unless otherwise noted.

³ Conformance to theoretical gain expression (see Equation 1 in the Theory of Operation section).

⁴ Conformance to best-fit dB linear curve.

⁵ For supplies greater than ±3.3 V, the operating temperature range is limited to –40°C ≤ T_A ≤ +85°C.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Voltage	
Supply Voltage (VPOS, VNEG)	± 6 V
Input Voltage (INPx)	VPOS, VNEG
Gain Voltage (GNHx, GNLO)	VPOS, VNEG
Power Dissipation	2.5 W
Temperature	
Operating Temperature Range	–40°C to +105°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C
Package Glass Transition Temperature (T_g)	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. The θ_{JA} values in Table 3 assume a 4-layer JEDEC standard board with zero airflow.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
40-Lead LFCSP ¹	31.0	2.3	°C/W

¹ 4-Layer JEDEC board (2S2P).

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation for the AD8264 is limited by the associated rise in junction temperature (T_j) on the die. At approximately 150°C, which is the glass transition temperature, the properties of the plastic change. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the amplifiers. Exceeding a temperature of 150°C for an extended period can cause changes in silicon devices, potentially resulting in a loss of functionality.

ESD CAUTION



ESD (electrostatic discharge) sensitive device.
Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

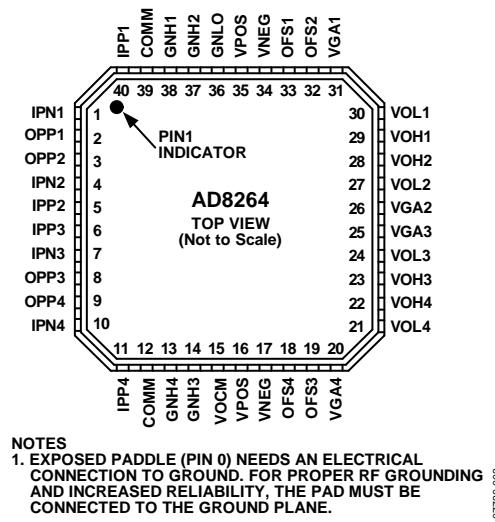


Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
0 (EP), 12, 39	COMM	Ground. Exposed paddle (EP, Pin 0) needs an electrical connection to ground. For proper RF grounding and increased reliability, the pad must be connected to the ground plane.
1, 4, 7, 10	IPN1, IPN2, IPN3, IPN4	Negative Preamp Inputs for Channel 1 Through Channel 4. Normally, no external connection is needed.
2, 3, 8, 9	OPP1, OPP2, OPP3, OPP4	Preamp Output for Channel 1 Through Channel 4. This pin is internally connected to the attenuator (VGA) input, and normally, no external connection is needed.
5, 6, 11, 40	IPP1, IPP2, IPP3, IPP4	Positive Preamp Input for Channel 1 Through Channel 4. High impedance.
13, 14, 37, 38	GNH1, GNH2, GNH3, GNH4	Positive Gain Control Voltage Input for Channel 1 Through Channel 4. This pin is referenced to GNLO (Pin 36).
15	VOCM	This pin sets the differential output amplifier (VOHx and VOLx) common-mode voltage.
16, 35	VPOS	Positive Supply (Internally Tied Together).
17, 34	VNEG	Negative Supply (Internally Tied Together).
18, 19, 32, 33	OFS1, OFS2, OFS3, OFS4	Voltage sets the differential output offset for Channel 1 through Channel 4. This is the noninverting input to the differential amplifier, and it has the same bandwidth as the inverting input (VGAx).
20, 25, 26, 31	VGA4, VGA3, VGA2, VGA1	VGA Output for Channel 1 Through Channel 4.
21, 24, 27, 30	VOL1, VOL2, VOL3, VOL4	Negative Differential Amplifier Output for Channel 1 Through Channel 4.
22, 23, 28, 29	VOH1, VOH2, VOH3, VOH4	Positive Differential Amplifier Output for Channel 1 Through Channel 4.
36	GNLO	Negative Gain Control Input (Reference for GNHx Pins).

TYPICAL PERFORMANCE CHARACTERISTICS

$V_S = \pm 2.5$ V, $T_A = 25^\circ\text{C}$, $f = 10$ MHz, $C_L = 5$ pF, $R_L = 500 \Omega$ per output (VGAx, VOHx, VOLx), $V_{\text{GAIN}} = (V_{\text{GNHx}} - V_{\text{GNLO}}) = 0$ V, $V_{\text{VOCM}} = \text{GND}$, $V_{\text{OFFS}} = \text{GND}$, gain range = 6 dB to 30 dB, unless otherwise specified.

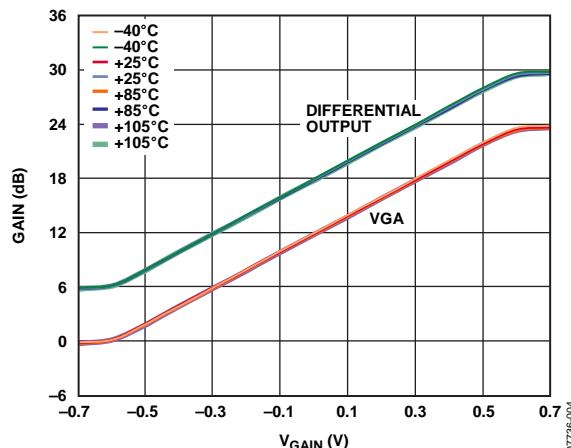
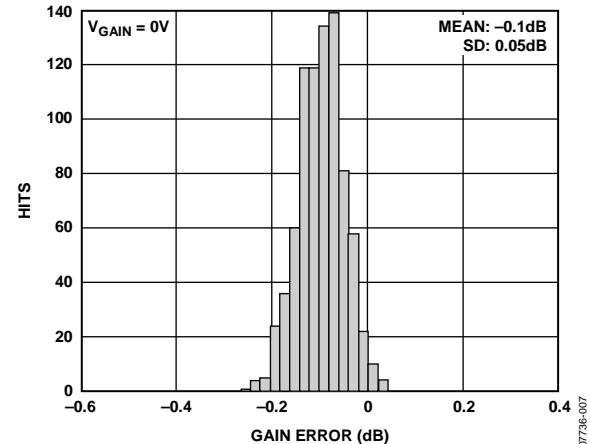
Figure 3. Gain vs. V_{GAIN} vs. Temperature

Figure 6. VGA Absolute Gain Error Histogram

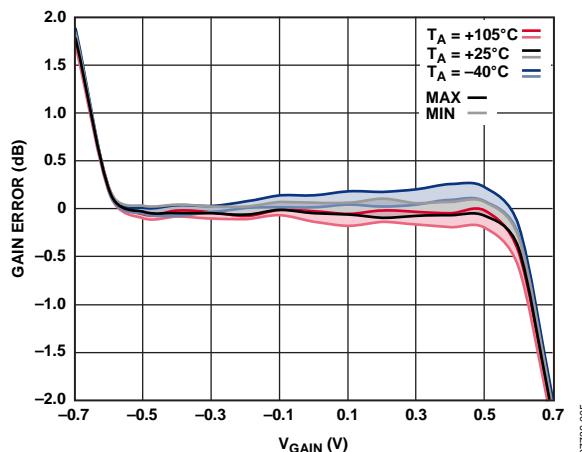
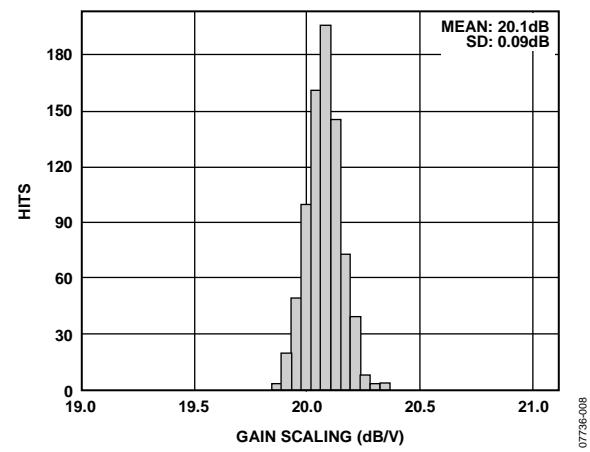
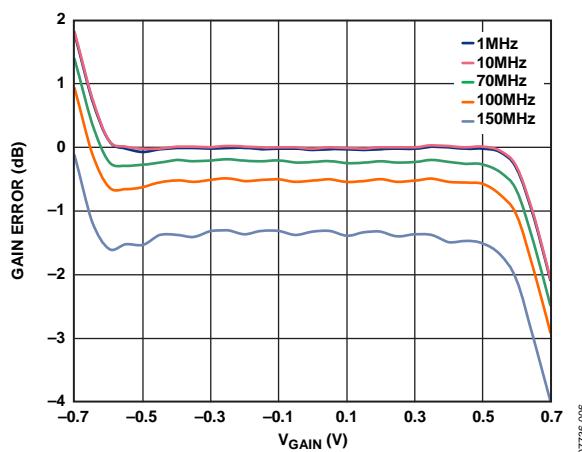
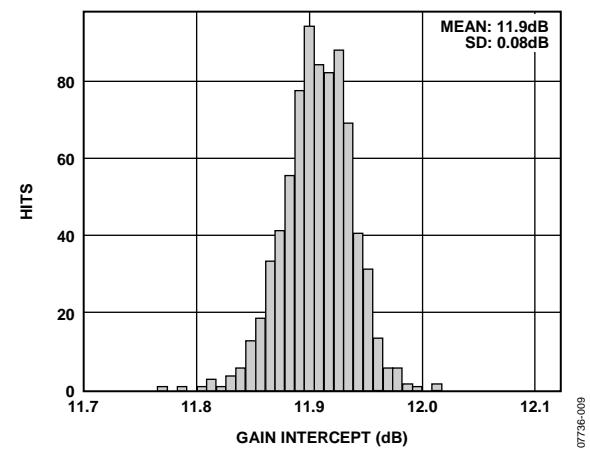
Figure 4. Gain Error vs. V_{GAIN} vs. TemperatureFigure 7. Gain Scale Factor Histogram ($-0.4 \text{ V} < V_{\text{GAIN}} < +0.4 \text{ V}$)Figure 5. Gain Error vs. V_{GAIN} at Various Frequencies to VGAx

Figure 8. VGA Gain Intercept Histogram

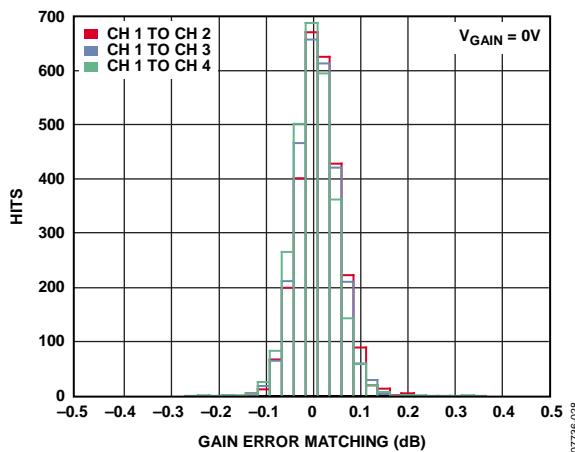


Figure 9. Channel-to-Channel Gain Match Histogram

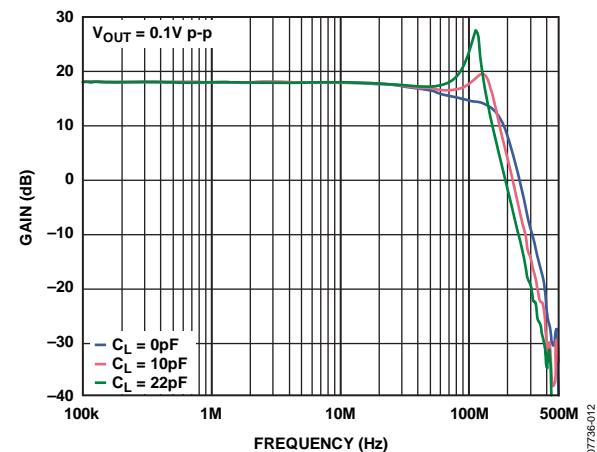


Figure 12. Frequency Response to Differential Output for Various Capacitive Loads

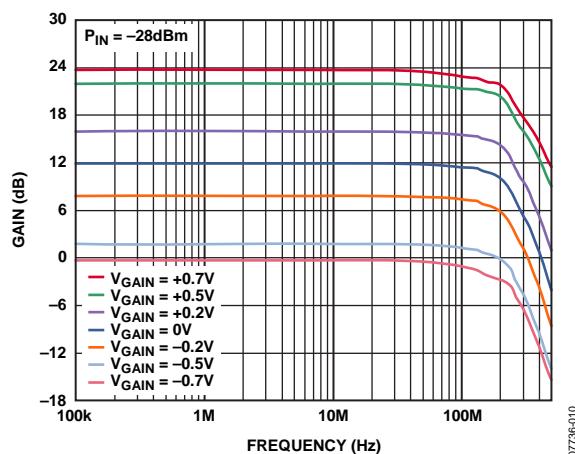
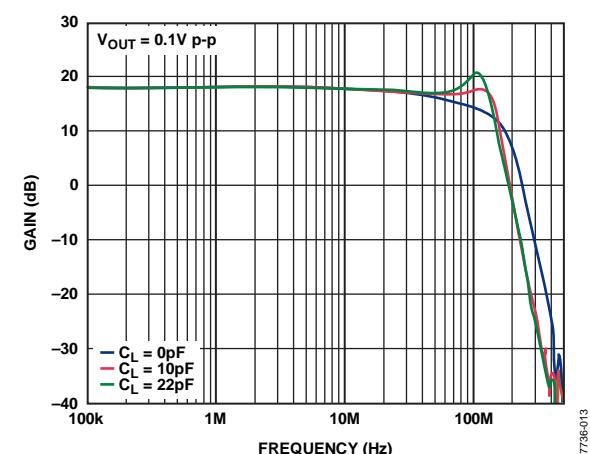
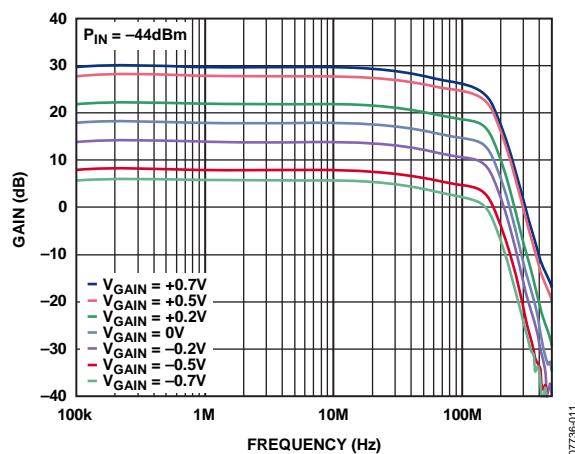
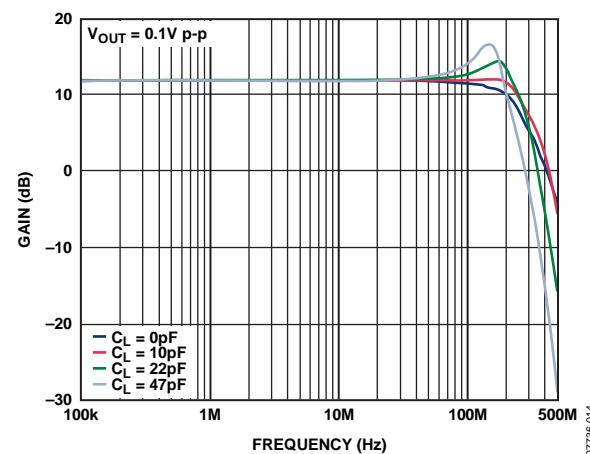
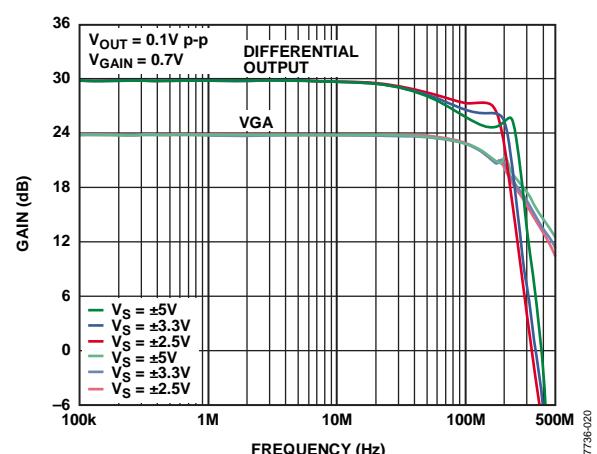
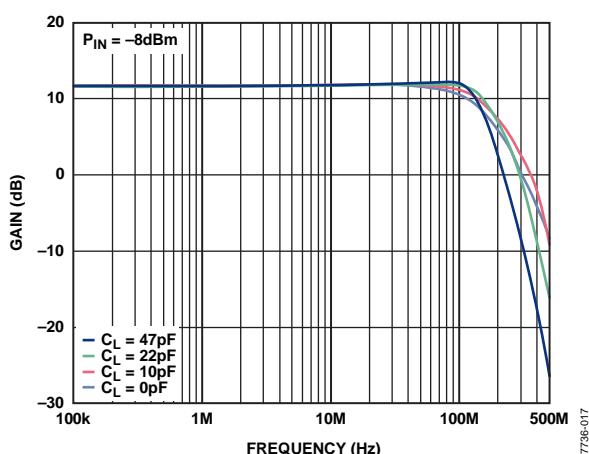
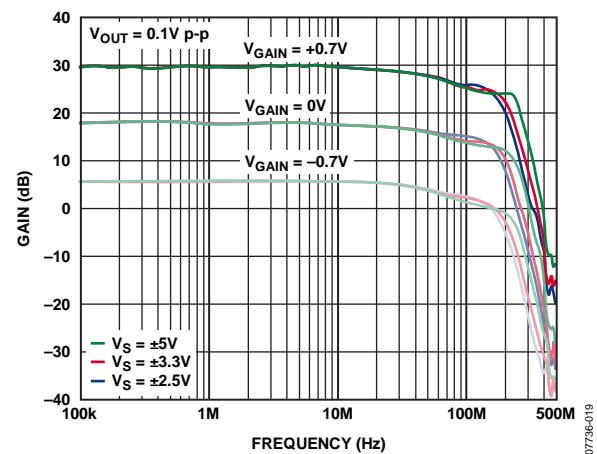
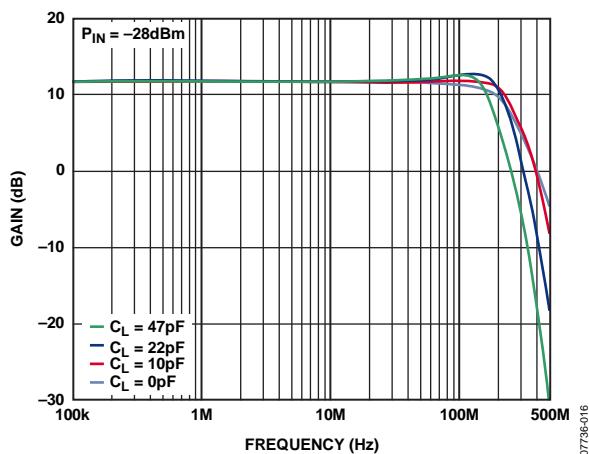
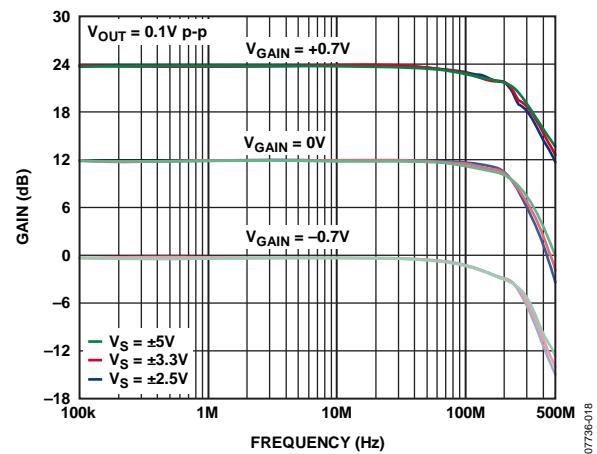
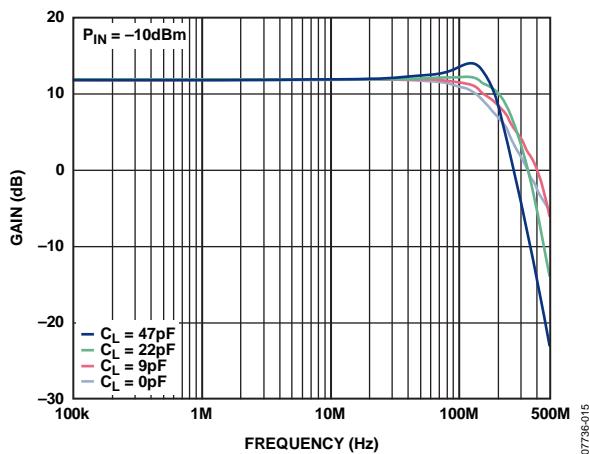
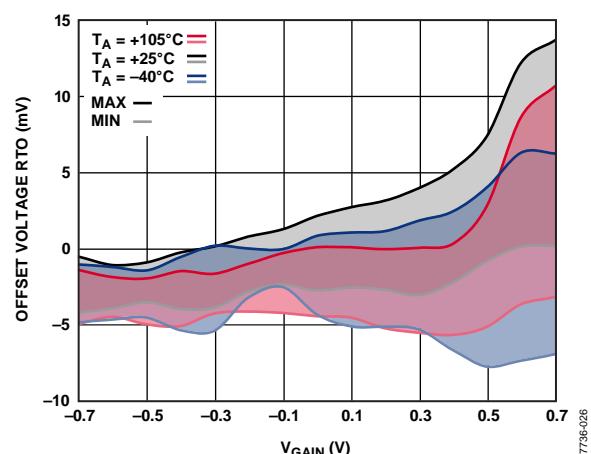
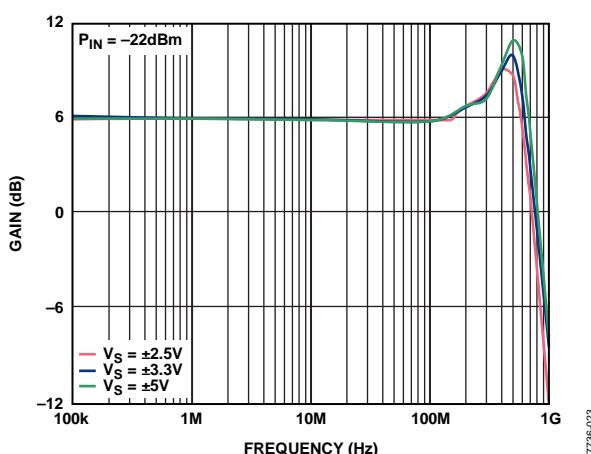
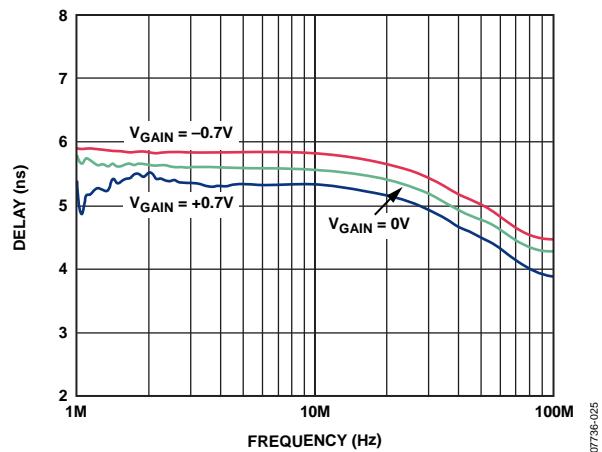
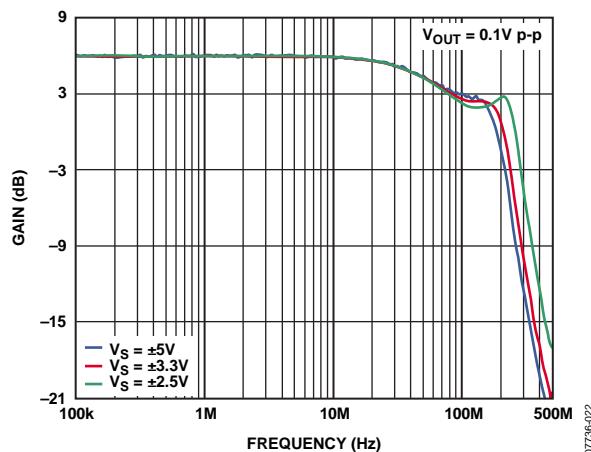
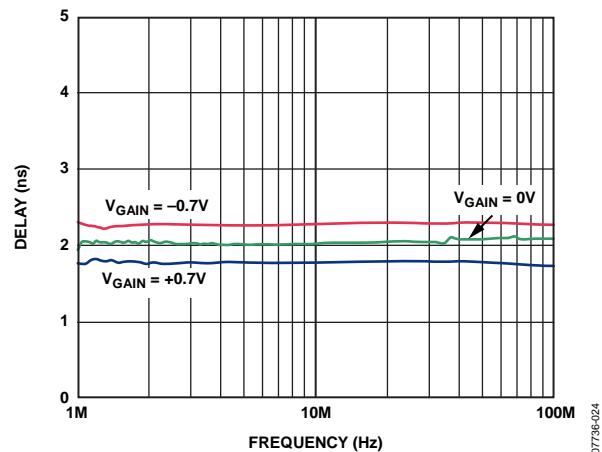
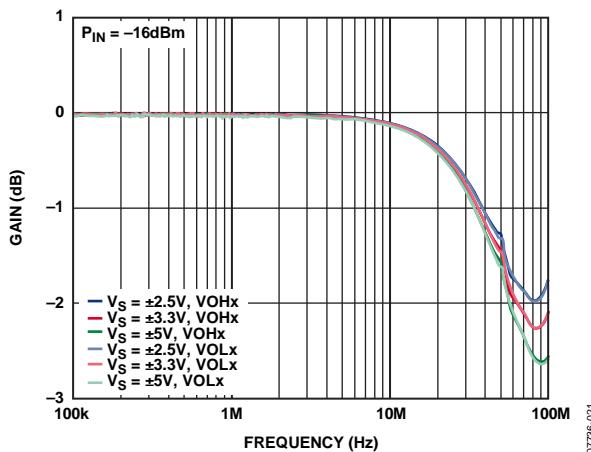
Figure 10. Frequency Response vs. Gain to VGAx for Various Values of V_{GAIN} Figure 13. Frequency Response to Differential Output for Various Capacitive Loads with Series $R = 10 \Omega$ Figure 11. Frequency Response vs. Gain to Differential Output for Various Values of V_{GAIN} 

Figure 14. Small Signal Frequency Response to VGAx for Various Capacitive Loads





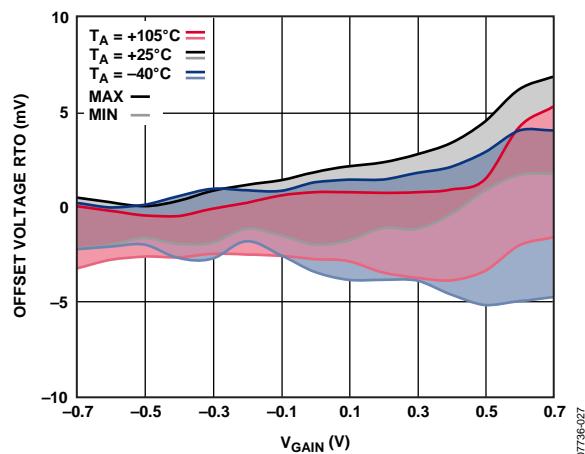


Figure 27. VGAx Output Offset Voltage vs. V_{GAIN} vs. Temperature

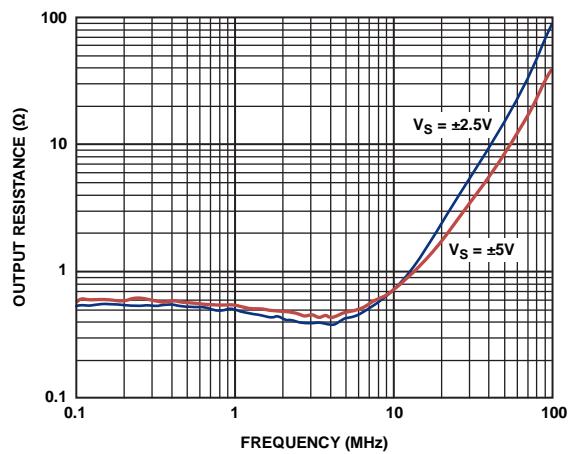


Figure 30. Output Resistance (VOHx, VOLx) vs. Frequency

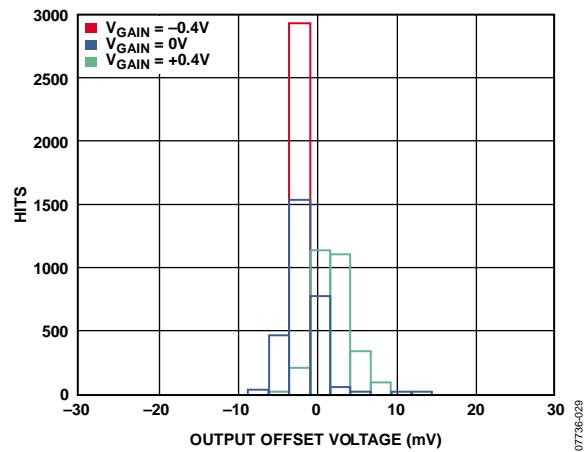


Figure 28. Output Offset Histogram to VGAx

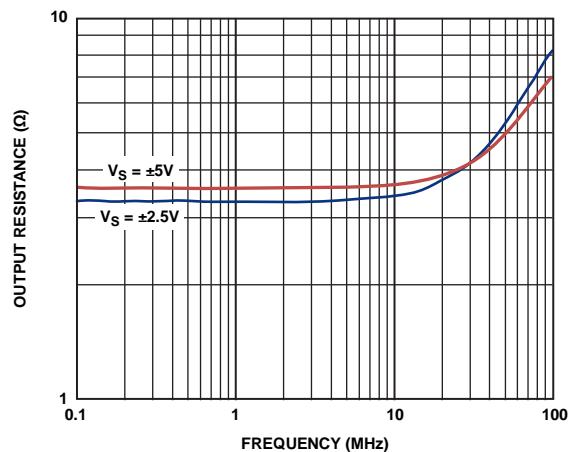


Figure 31. Output Resistance (VGAx) vs. Frequency

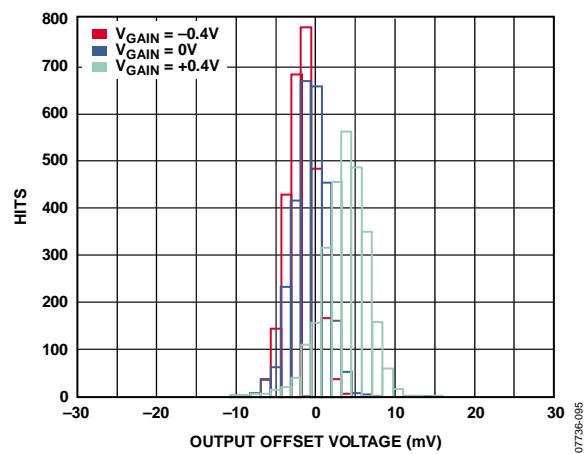


Figure 29. Output Offset Histogram to Differential Output

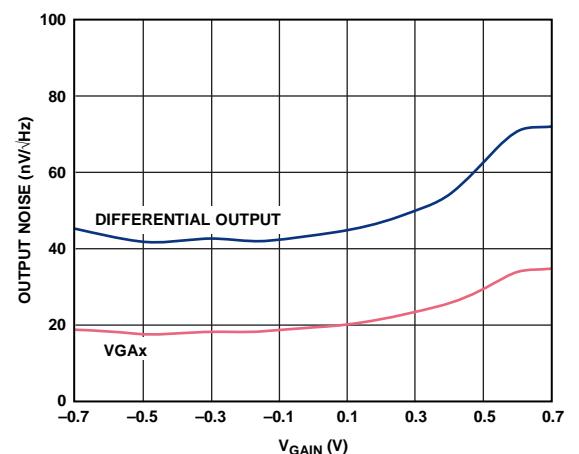
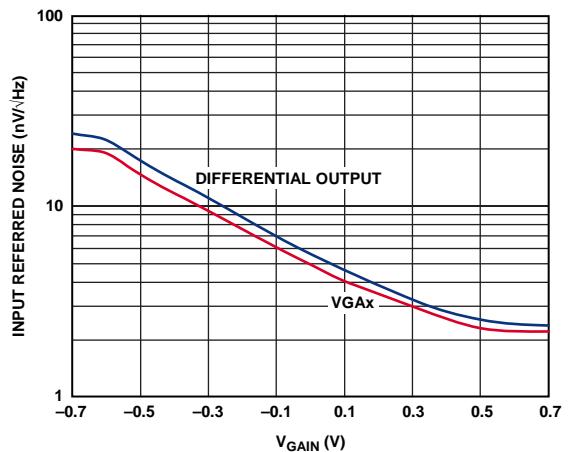
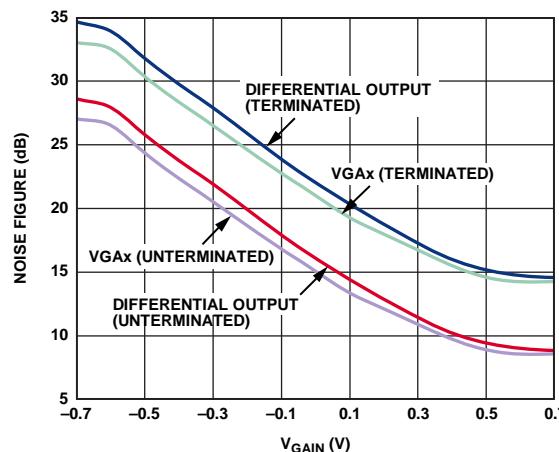


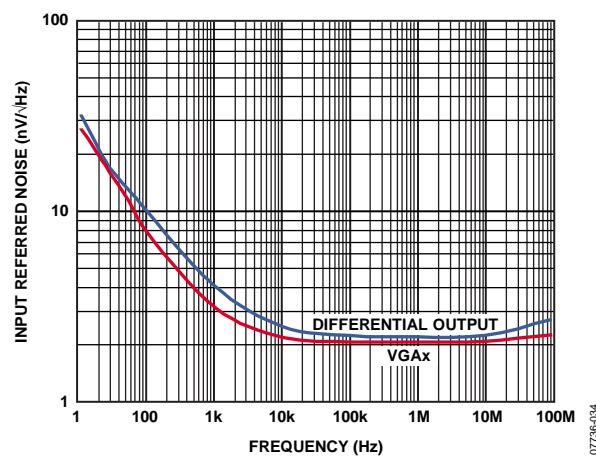
Figure 32. Output Referred Noise to VGAx and Differential Output vs. V_{GAIN}



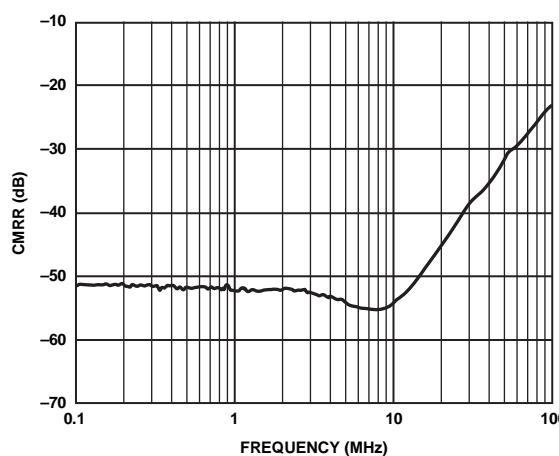
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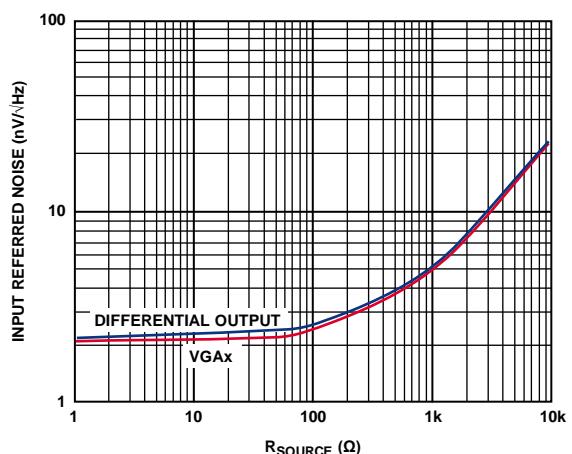
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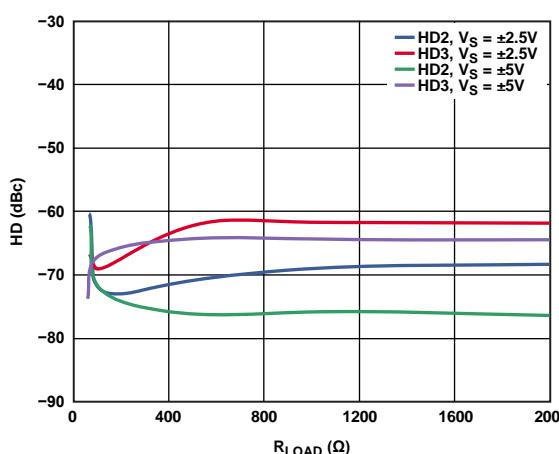
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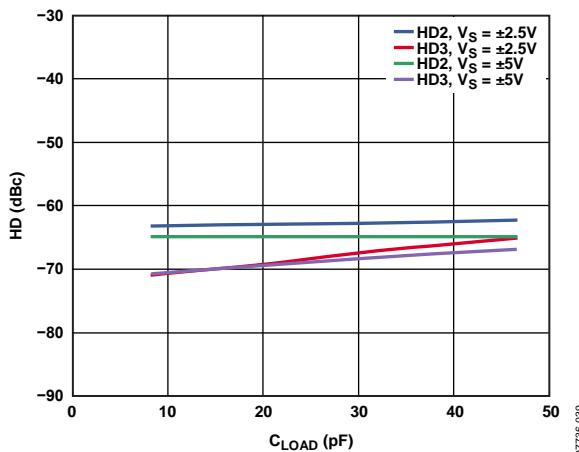
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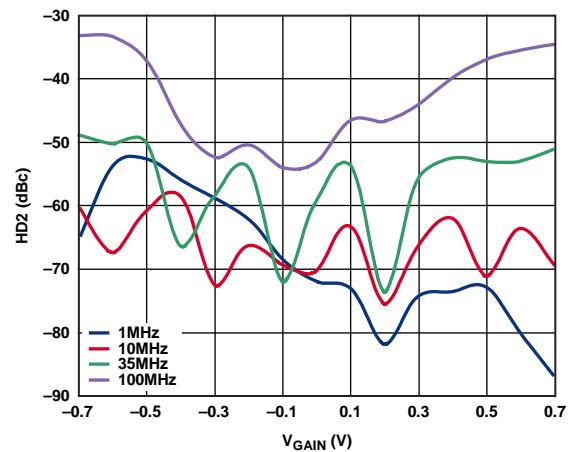
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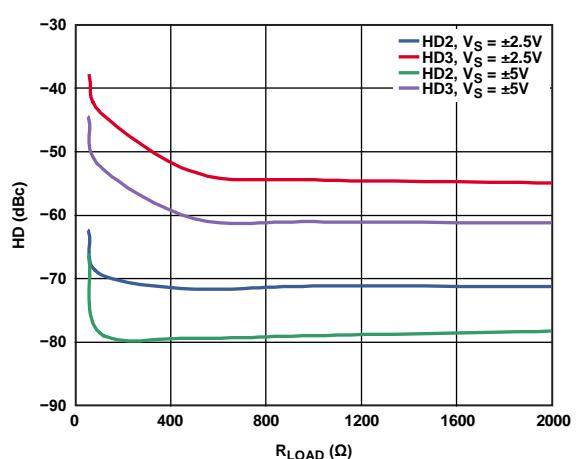
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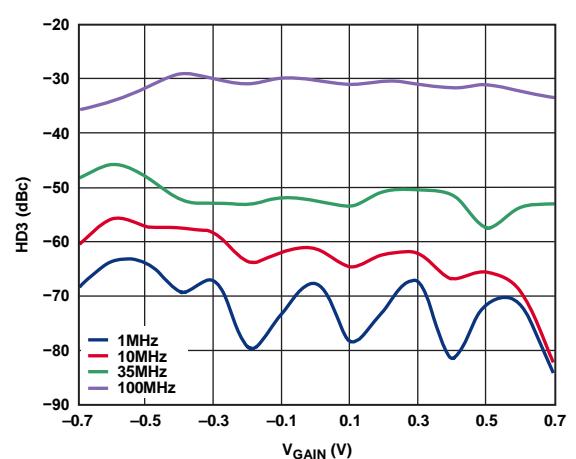
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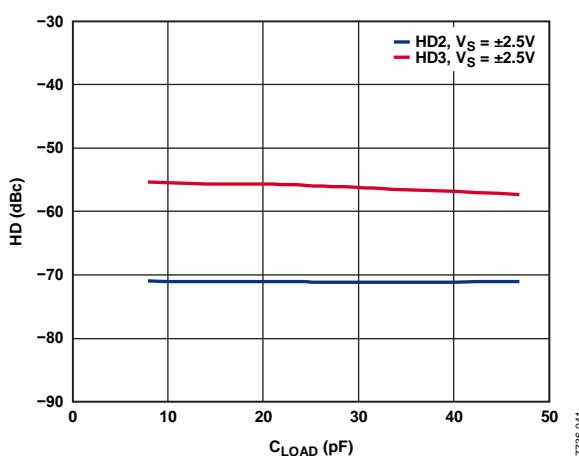
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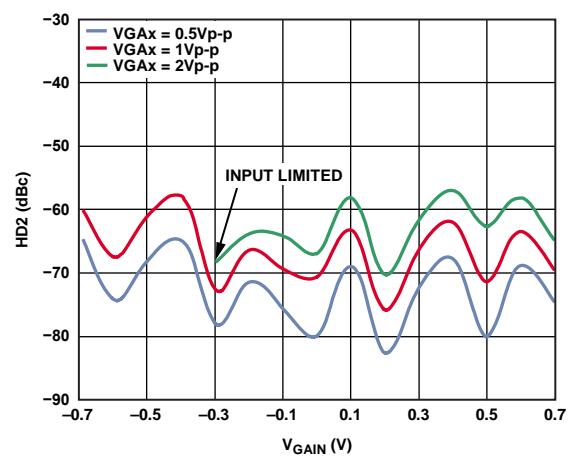
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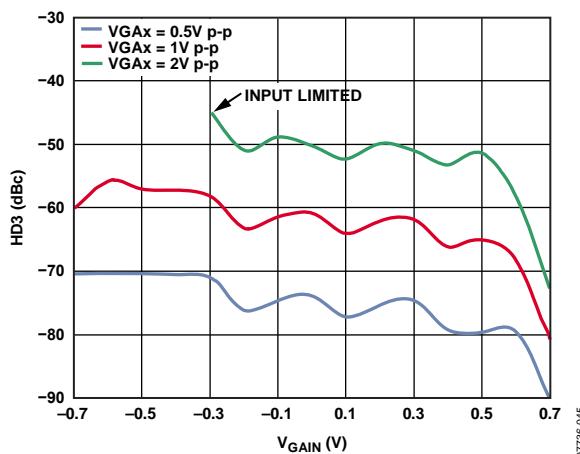
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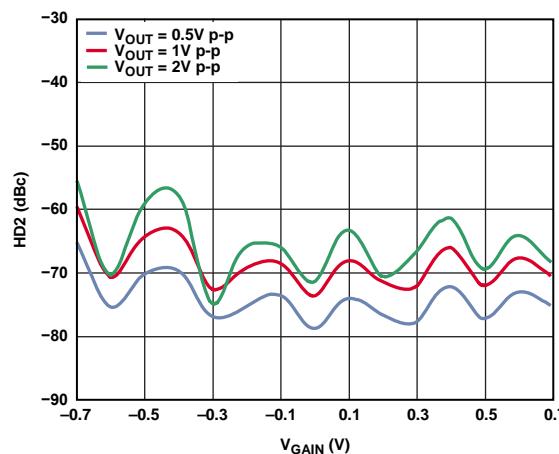
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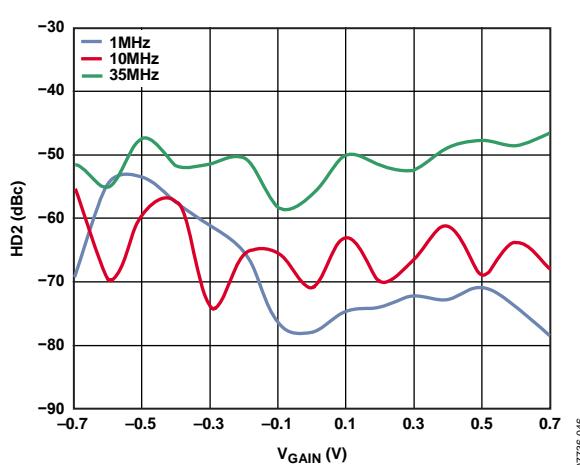
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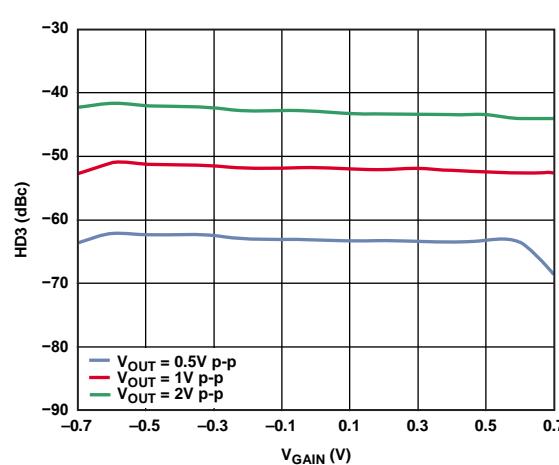
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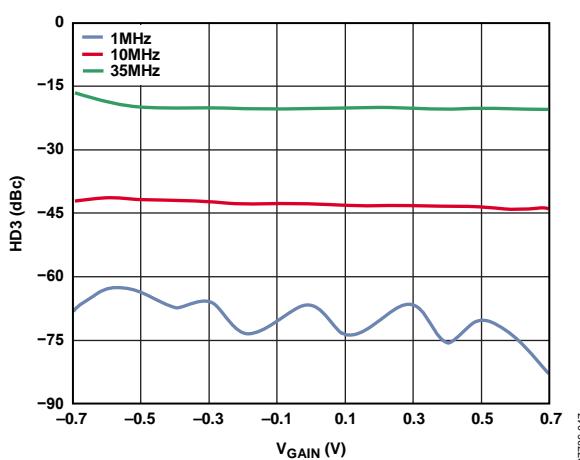
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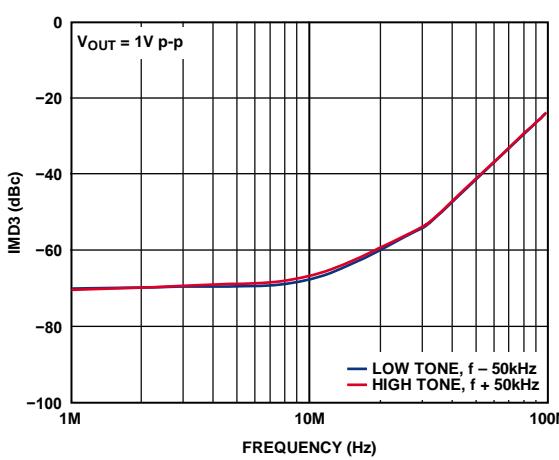
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07738-049



07738-047



07738-050

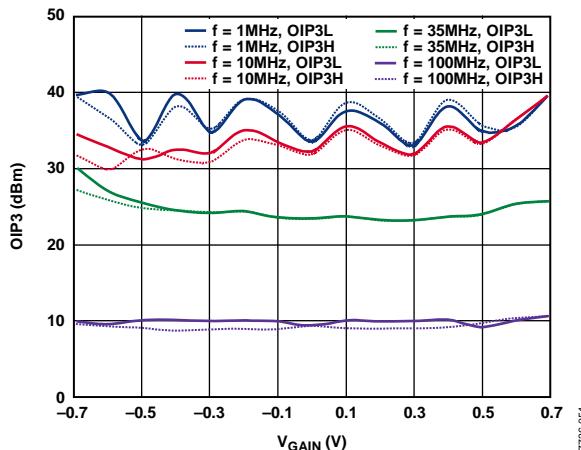


Figure 51. OIP3 vs. V_{GAIN} vs. Frequency to VGAx

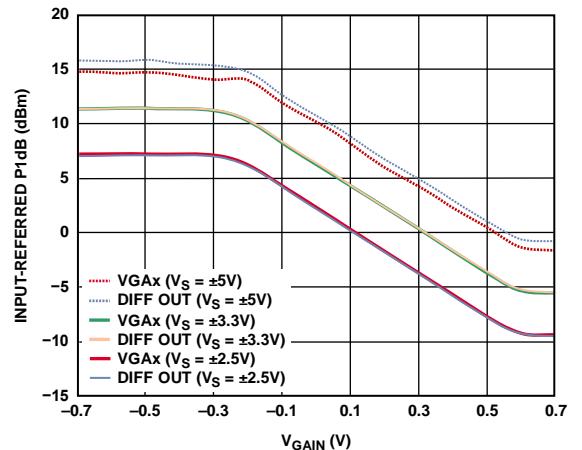


Figure 54. Input P1dB vs. V_{GAIN}

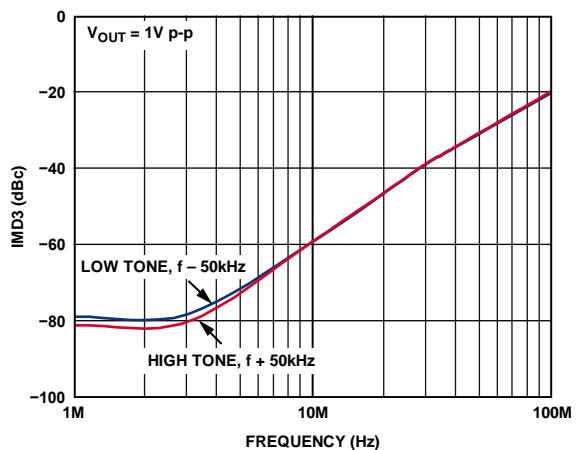


Figure 52. IMD3 vs. Frequency to Differential Output

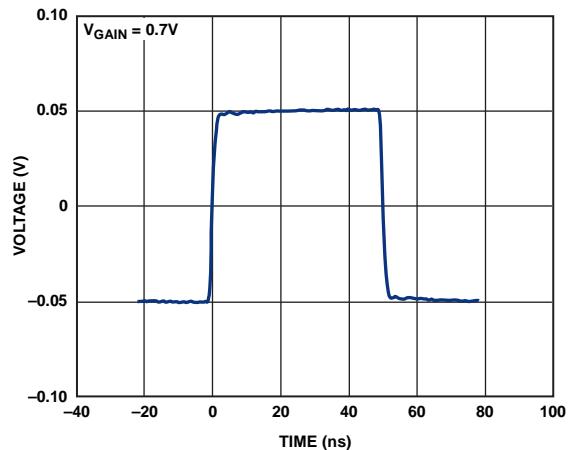


Figure 55. Small Signal Pulse Response to VGAx

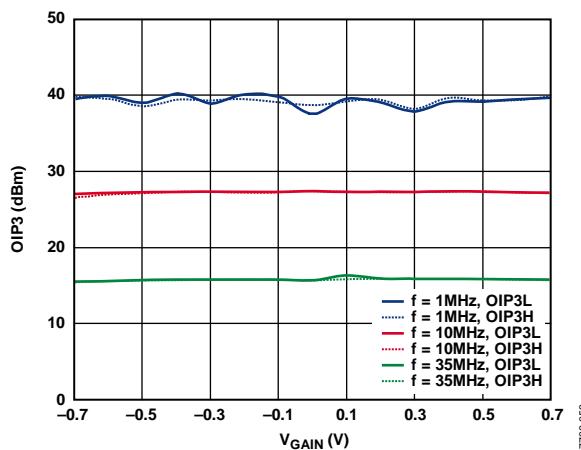


Figure 53. OIP3 vs. Frequency to Differential Output

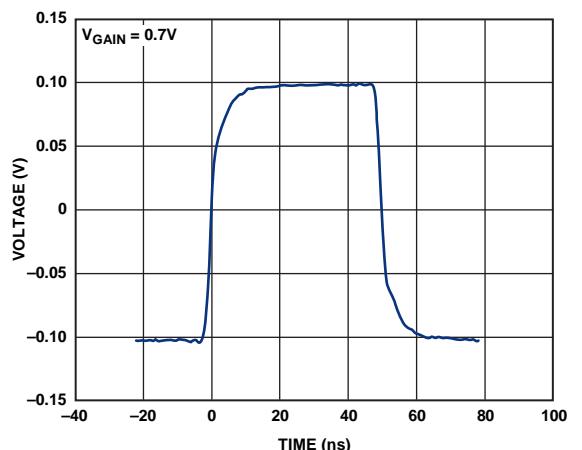
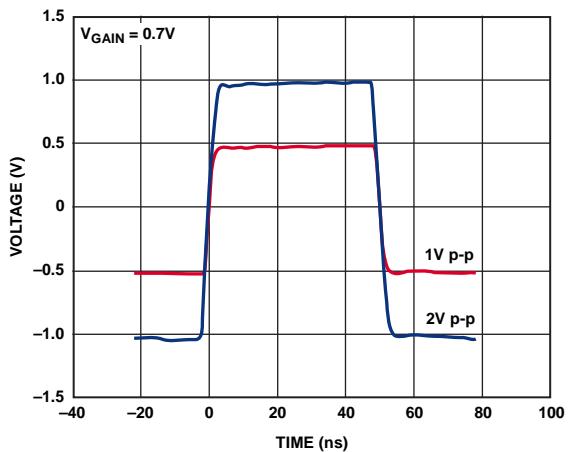
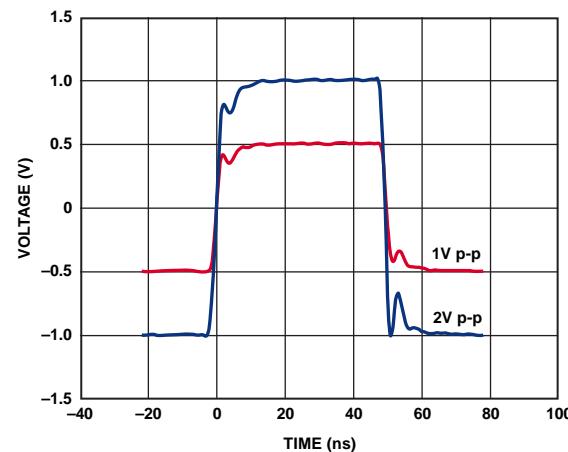


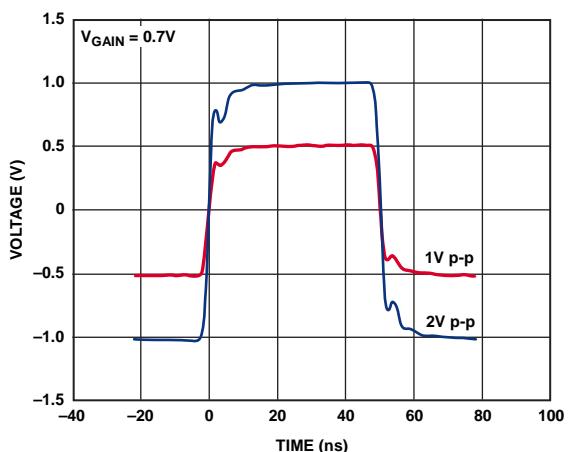
Figure 56. Small Signal Pulse Response to Differential Output



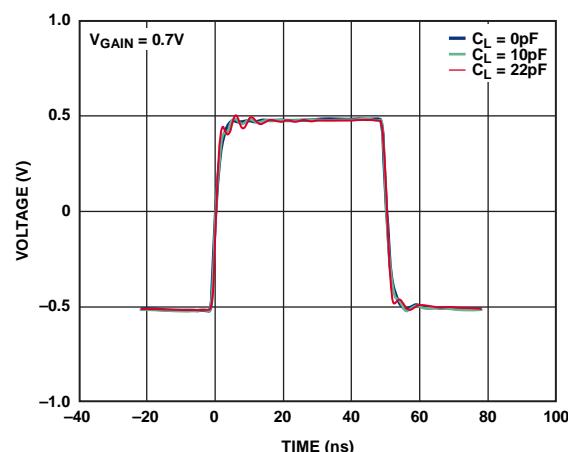
07738-057



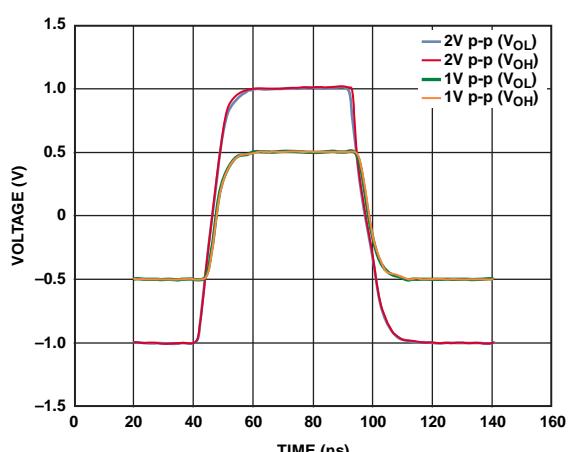
07738-060



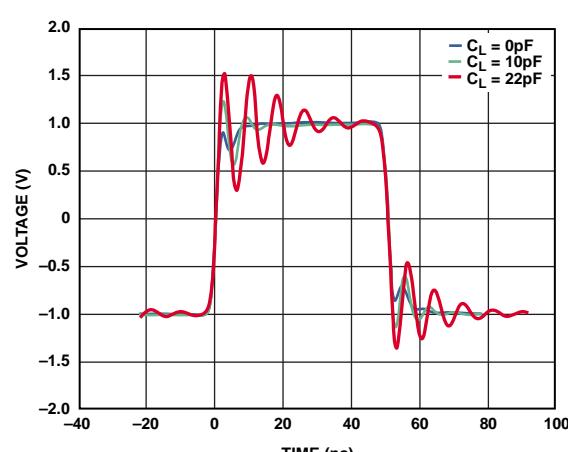
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07738-061



07738-059



07738-062

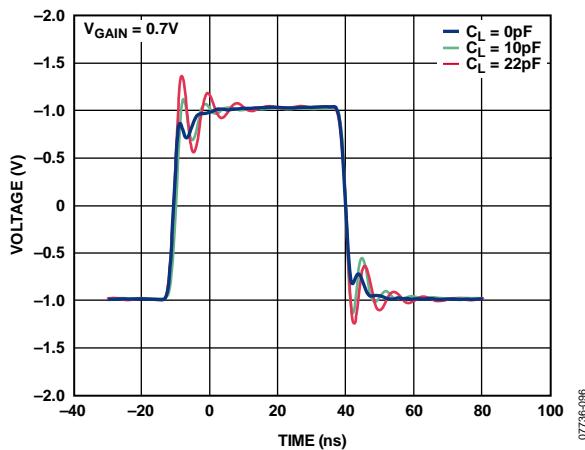


Figure 63. Large Signal Pulse Response to Differential Output for Various Capacitive Loads with Series $R = 10 \Omega$

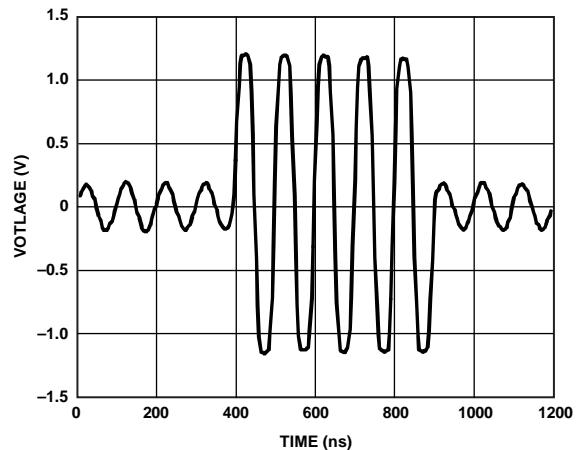


Figure 66. Preamp Overdrive Recovery

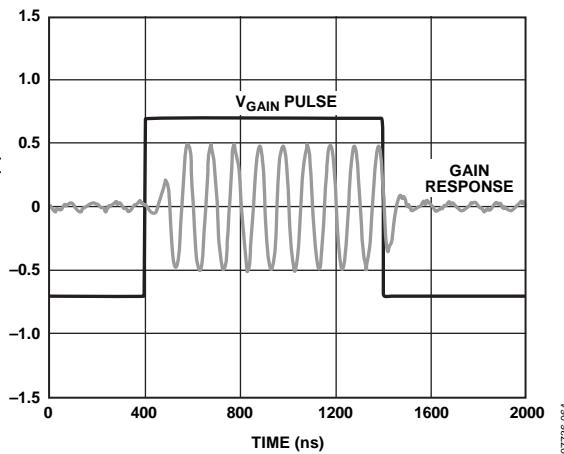


Figure 64. VGAx Response to Change in V_{GAIN}

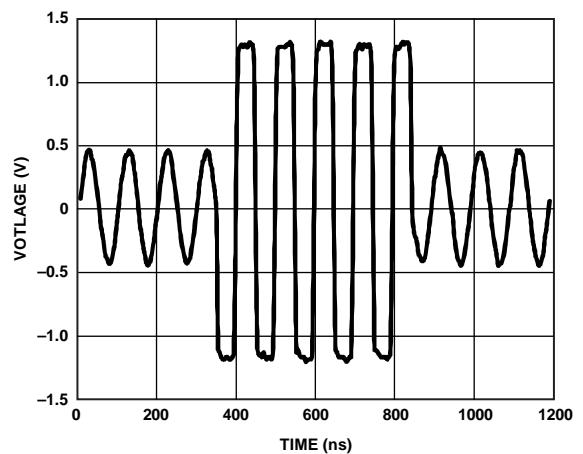


Figure 67. VGA Overdrive Recovery

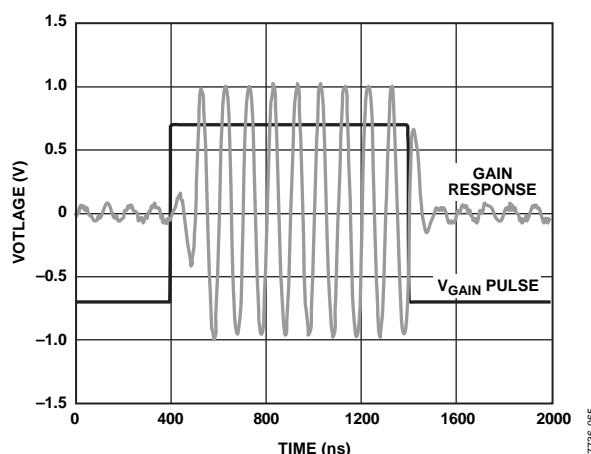


Figure 65. Differential Output Response to Change in V_{GAIN}

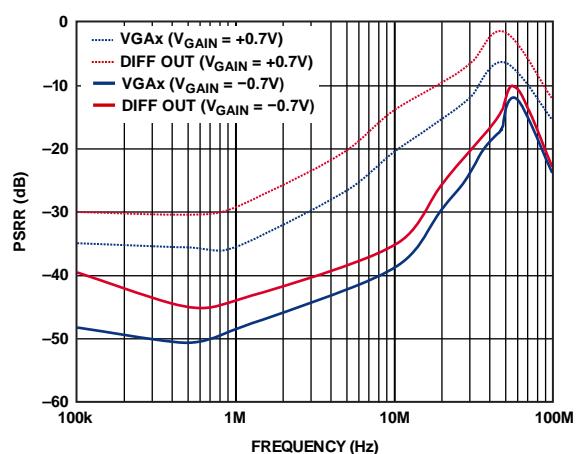
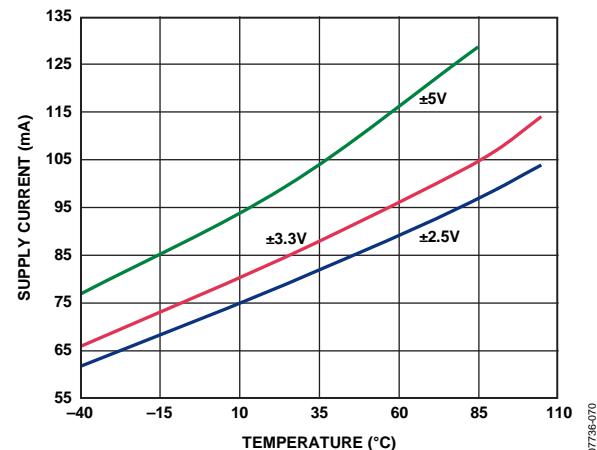
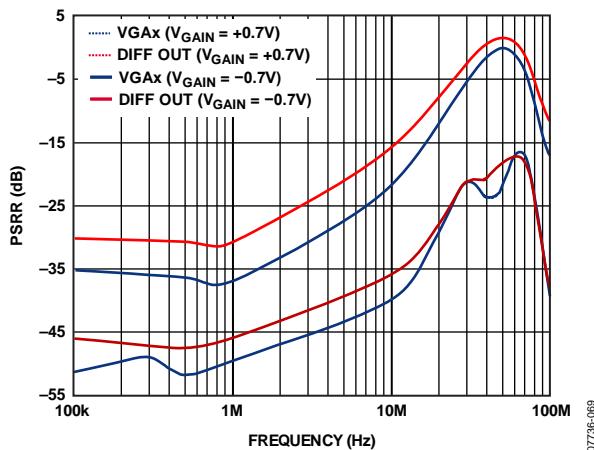


Figure 68. Power Supply Rejection vs. Frequency (VPOS)



TEST CIRCUITS

$V_S = \pm 2.5$ V, $T_A = 25^\circ\text{C}$, $f = 10$ MHz, $C_L = 5$ pF, $R_L = 500 \Omega$ per output (VGAx, VOHx, VOLx), $V_{\text{GAIN}} = (V_{\text{GNHx}} - V_{\text{GNLo}}) = 0$ V, $V_{\text{VOCM}} = \text{GND}$, $V_{\text{OFSx}} = \text{GND}$, gain range = 6 dB to 30 dB, unless otherwise specified.

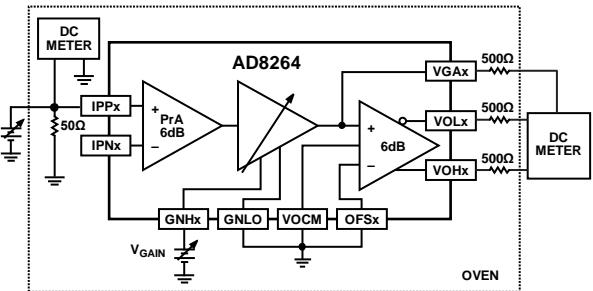


Figure 71. Gain vs. V_{GAIN} vs. Temperature (See Figure 3 and Figure 4)

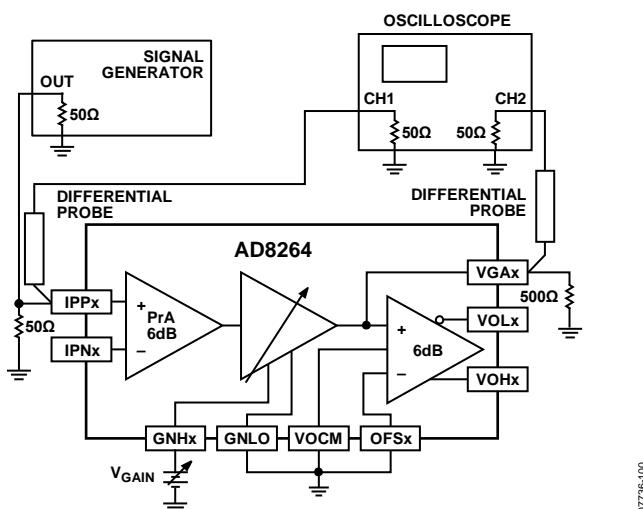


Figure 72. Gain Error vs. V_{GAIN} at Various Frequencies to VGAx (See Figure 5)

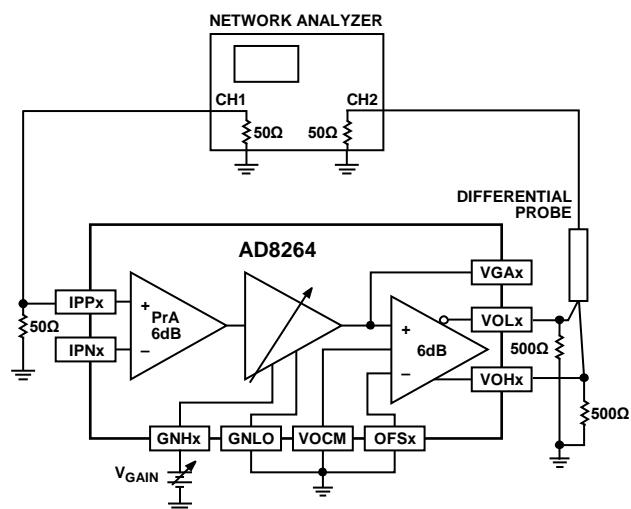


Figure 74. Frequency Response vs. Gain to Differential Output for Various Values of V_{GAIN} (See Figure 11)

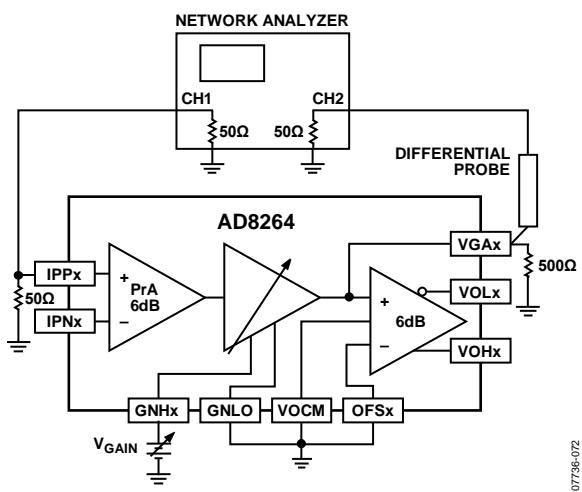


Figure 73. Frequency Response vs. Gain to VGAx for Various Values of V_{GAIN}
 $V_{\text{GAIN}} = V_{\text{GNHx}} - V_{\text{GNLo}}$ (See Figure 10)

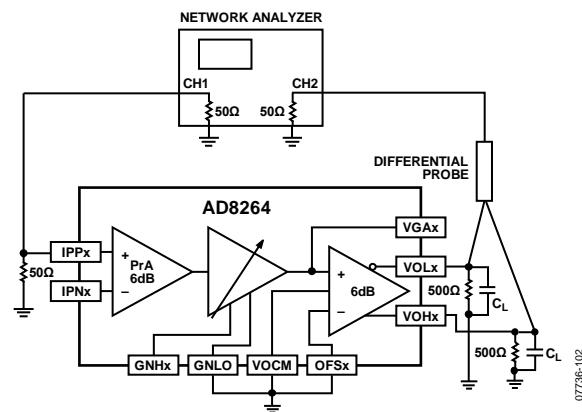


Figure 75. Frequency Response to Differential Output for Various Capacitive Loads (See Figure 12)

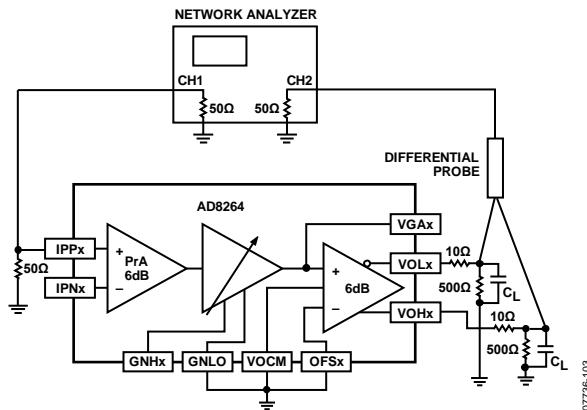


Figure 76. Frequency Response to Differential Output for Various Capacitive Loads with Series R = 10 Ω (See Figure 13)

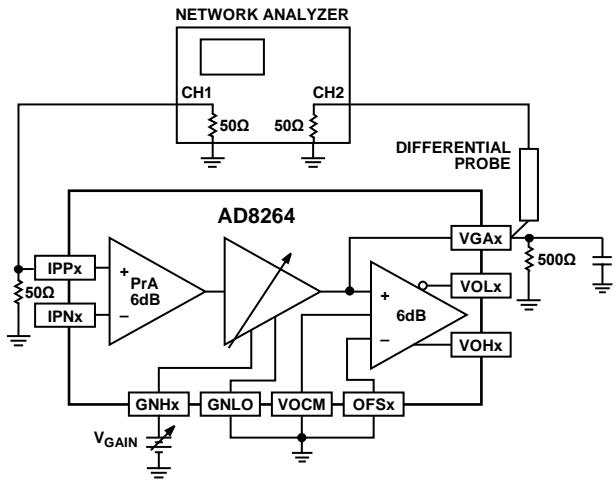


Figure 77. Frequency Response to VGAx for Various Capacitive Loads (See Figure 14)

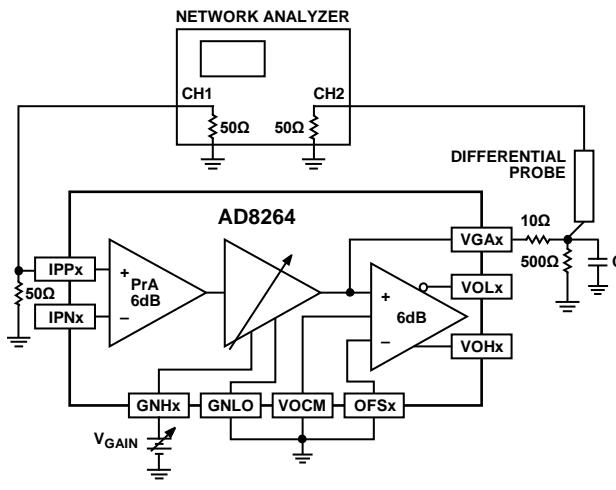


Figure 78. Frequency Response to VGAx for Various Capacitive Loads with Series R = 10 Ω (See Figure 16)

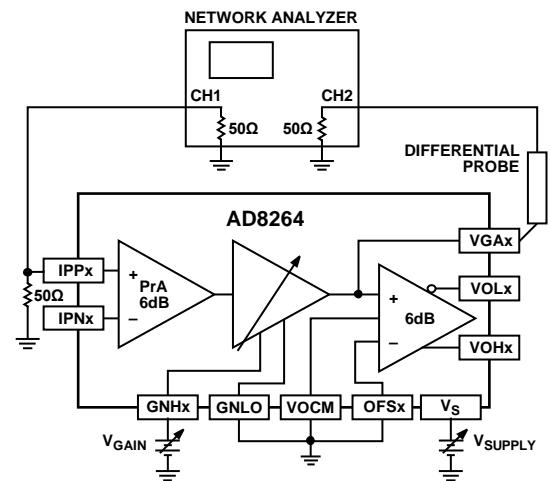


Figure 79. Frequency Response vs. Gain to VGAx for Various Supply Voltages (See Figure 18)

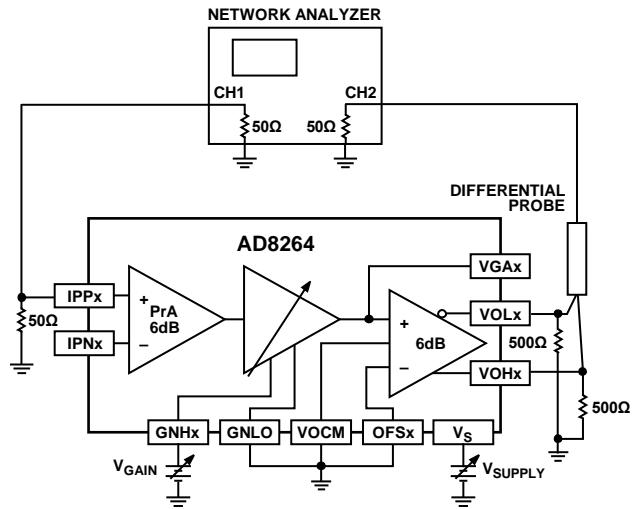


Figure 80. Frequency Response vs. Gain to Differential Output for Various Supply Voltages (See Figure 19)

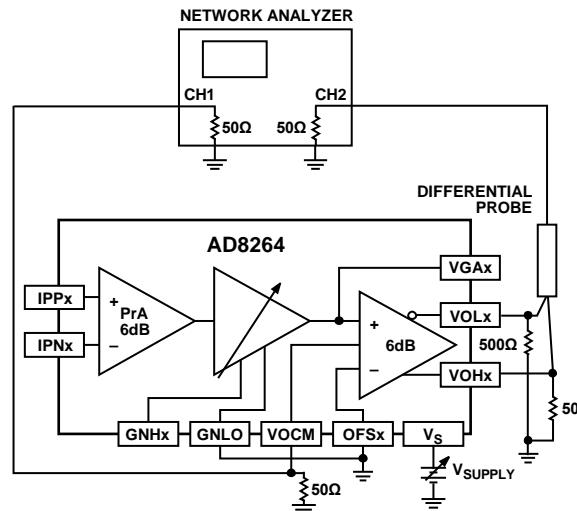


Figure 81. VOCM Frequency Response to Differential Output (See Figure 21)

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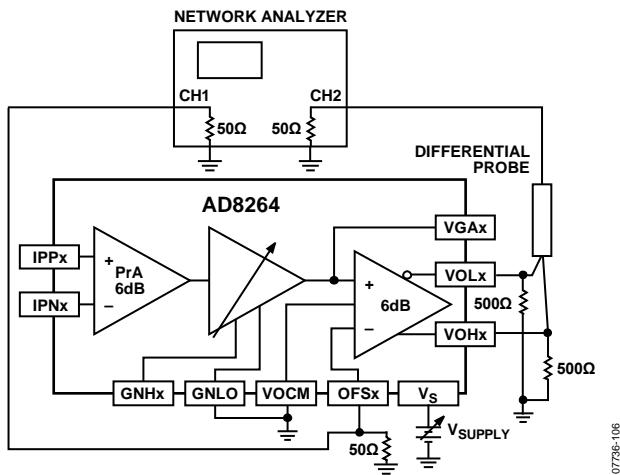


Figure 82. OFSx Frequency Response to Differential Output (See Figure 22)

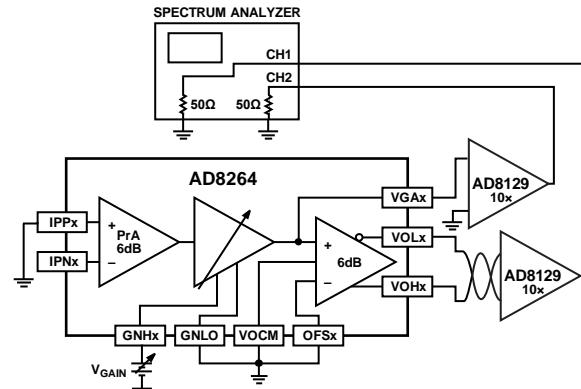


Figure 85. Output Referred Noise vs. V_{GAIN} (See Figure 32)

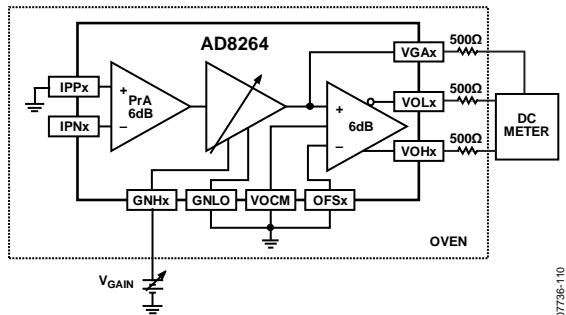


Figure 83. Output Offset Voltage vs. V_{GAIN} vs. Temperature (See Figure 26 and Figure 27)

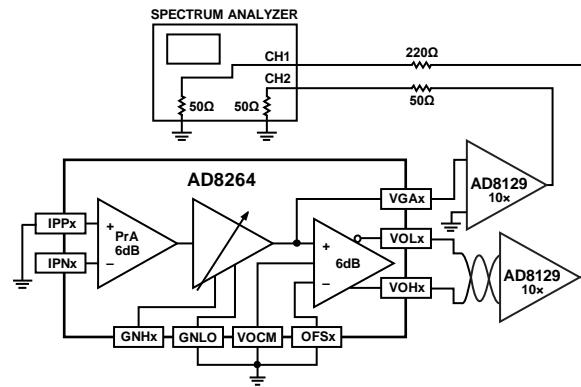


Figure 86. Input Referred Noise vs. Frequency (See Figure 34)

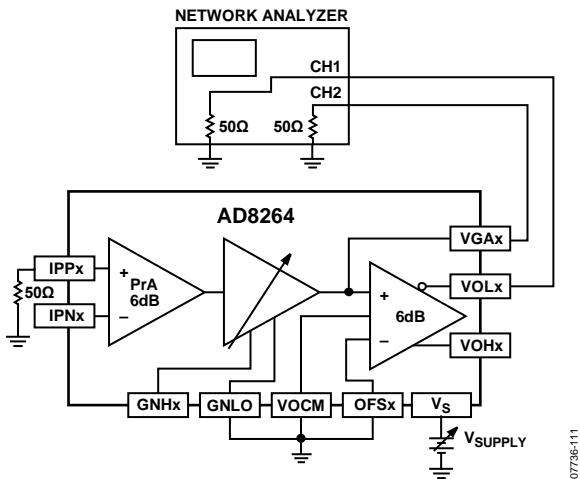


Figure 84. Output Resistance vs. Frequency (See Figure 30 and Figure 31)

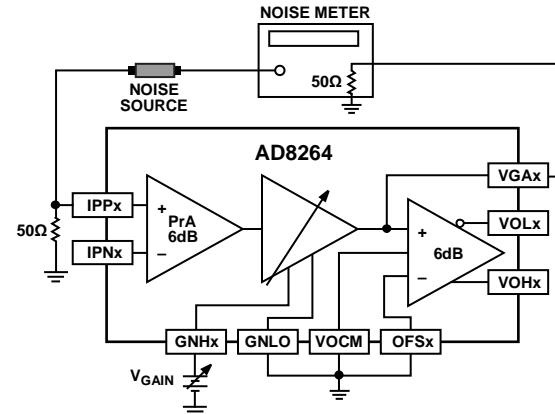
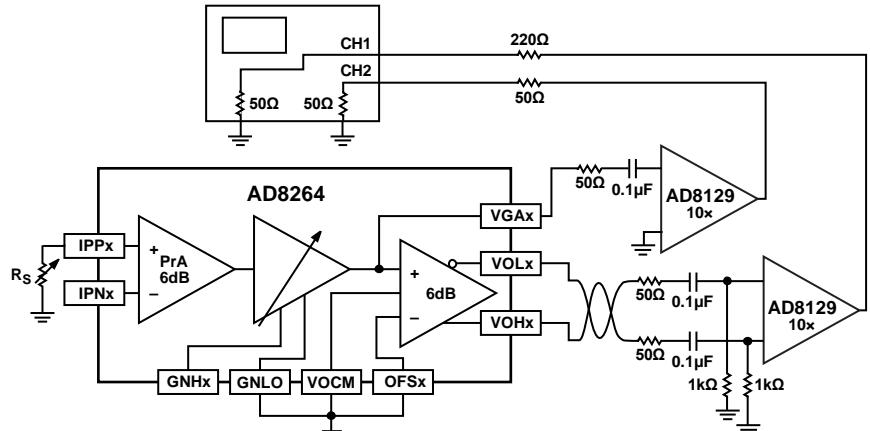


Figure 87. Noise Figure vs. V_{GAIN} (See Figure 36)

SPECTRUM ANALYZER

Figure 88. Input Referred Noise vs. R_{SOURCE} (See Figure 35)

NETWORK ANALYZER

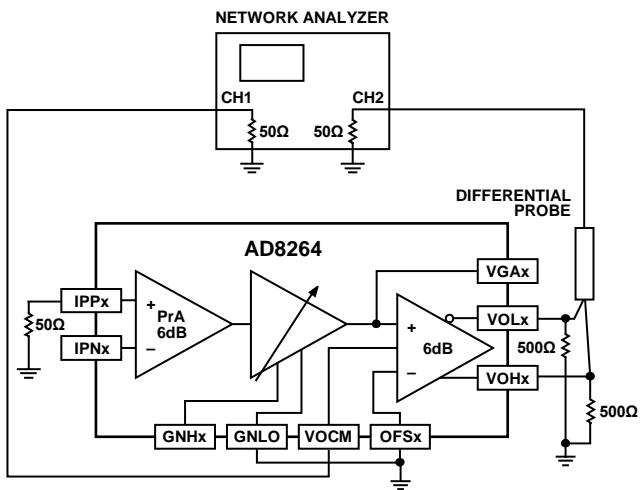
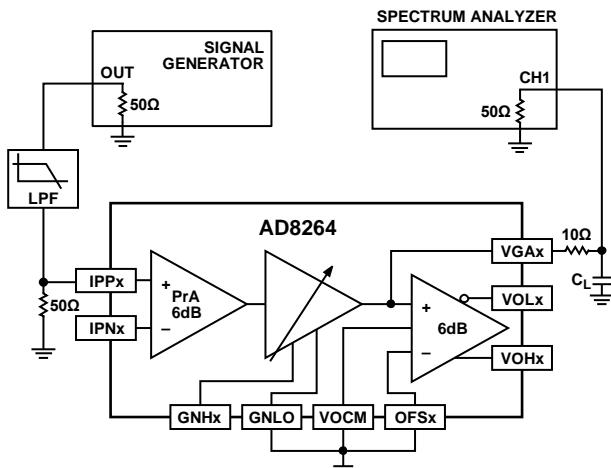
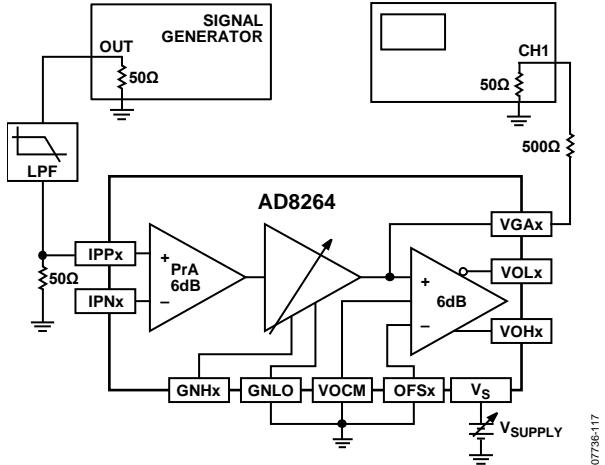


Figure 89. VOCM Common-Mode Rejection vs. Frequency (See Figure 37)

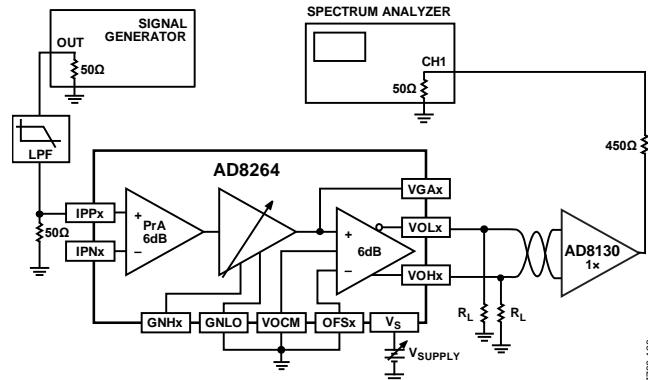
SPECTRUM ANALYZER

Figure 91. Harmonic Distortion to VGAx vs. C_{LOAD} (Figure 39)

SPECTRUM ANALYZER

Figure 90. Test Circuit Harmonic Distortion to VGAx vs. R_{LOAD} and Various Supplies (See Figure 38)

SPECTRUM ANALYZER

Figure 92. Harmonic Distortion to Differential Output vs. R_{LOAD} and Various Supplies (See Figure 40)

AD8264

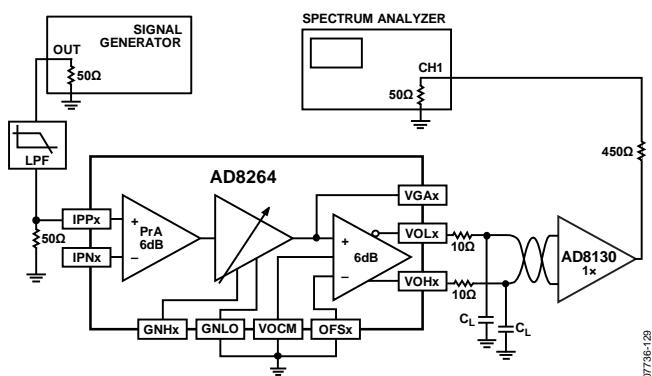


Figure 93. Harmonic Distortion to Differential Output vs.
 C_{LOAD} (See Figure 41)

07736-123

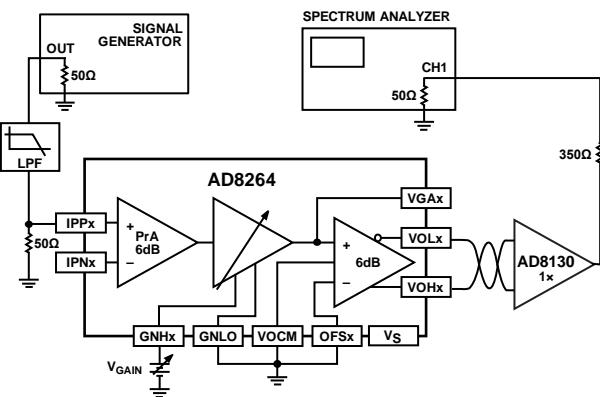


Figure 95. HD2 and HD3 to Differential Output (See Figure 46 through Figure 49)

07736-131

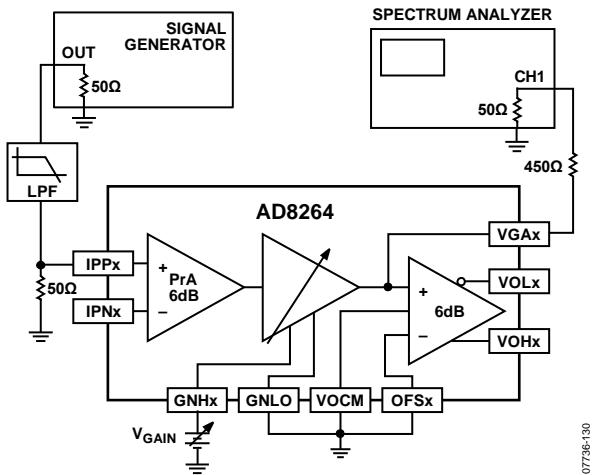


Figure 94. HD2 and HD3 to VGAx (See Figure 42 Through Figure 45)

07736-130

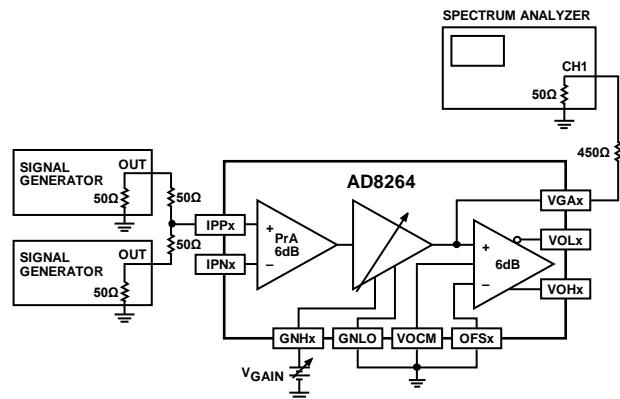


Figure 96. IMD3 and OIP3 to VGAx (See Figure 50 and Figure 51)

07736-132

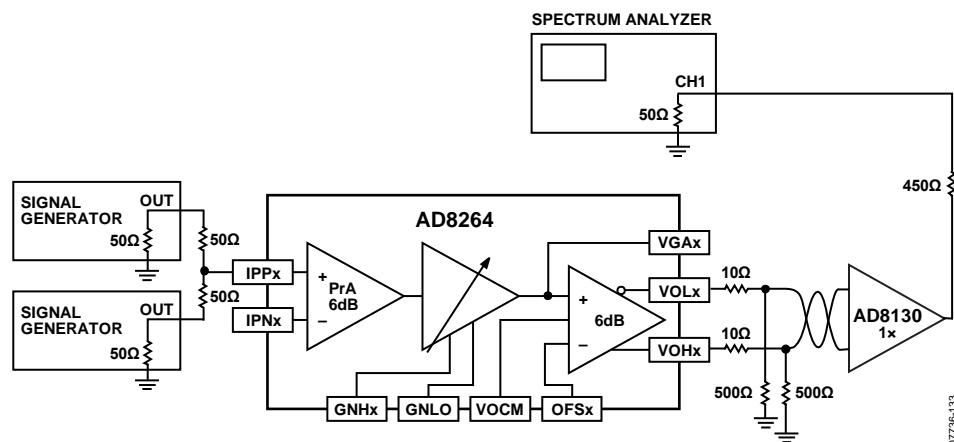


Figure 97. IMD3 and OIP3 to Differential Output (See Figure 52 and Figure 53)

07736-133

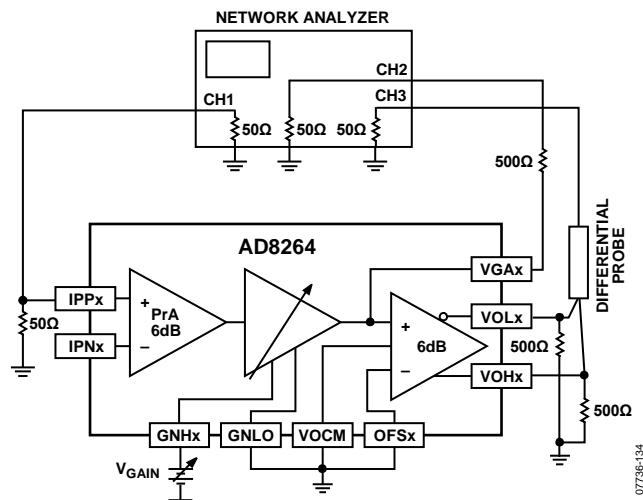
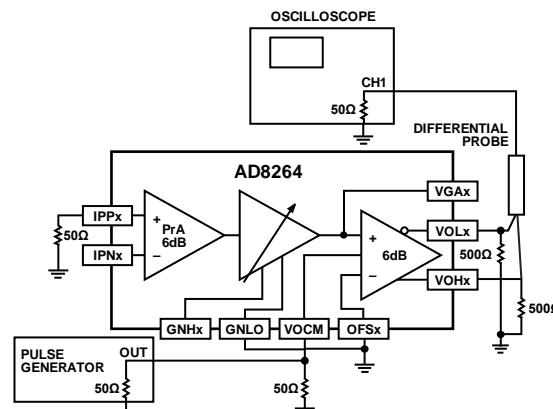
Figure 98. Input P1dB vs. V_{GAIN} (See Figure 54)

Figure 101. VOCM Pulse Response (See Figure 59)

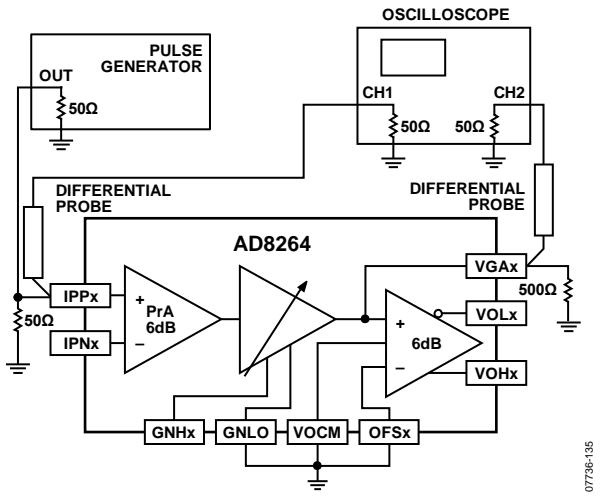
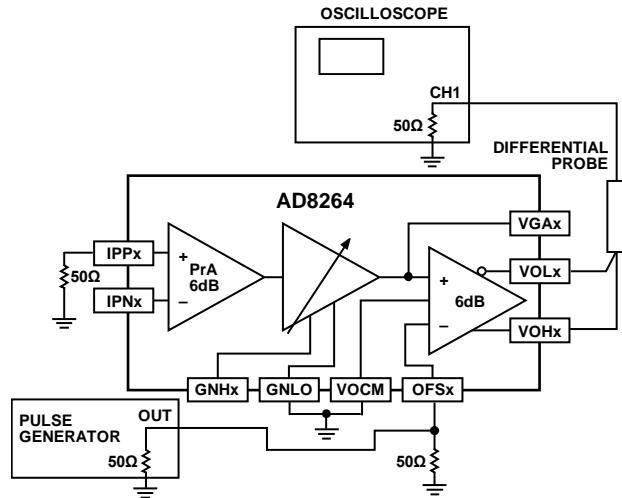
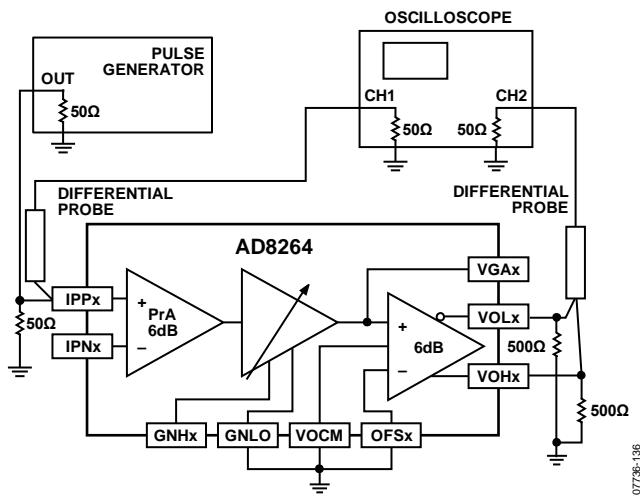
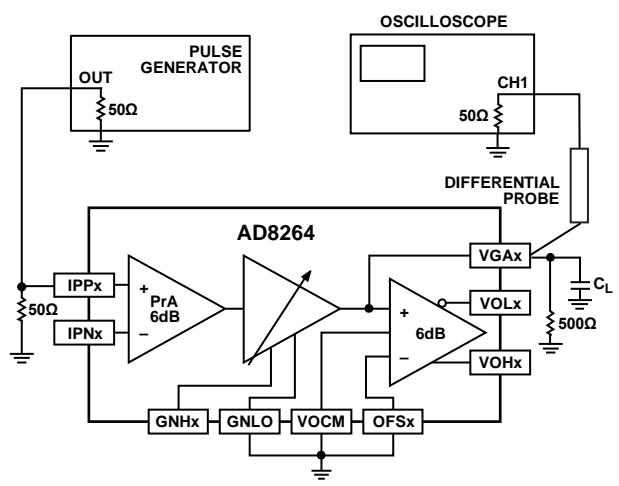
Figure 99. Pulse Response to VG_{Ax} , $V_{GAIN} = 0.7$ V (See Figure 55 and Figure 57)

Figure 102. OFSx Pulse Response (See Figure 60)

Figure 100. Pulse Response to Differential Outputs, $V_{GAIN} = 0.7$ V (See Figure 56 and Figure 58)Figure 103. Pulse Response to VG_{Ax} for Various Capacitive Loads, $V_{GAIN} = 0.7$ V (See Figure 61)

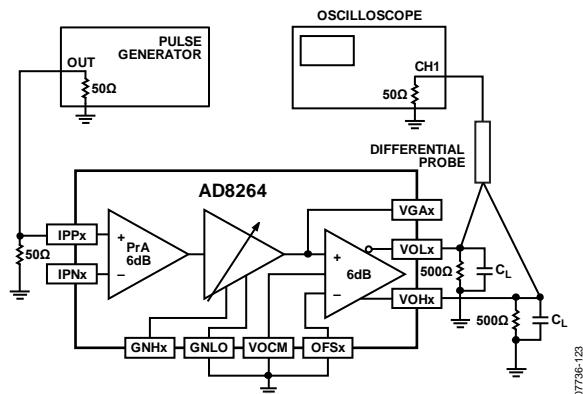


Figure 104. Pulse Response to Differential Output for Various Capacitive Loads, $V_{GAIN} = 0.7$ V (See Figure 62)

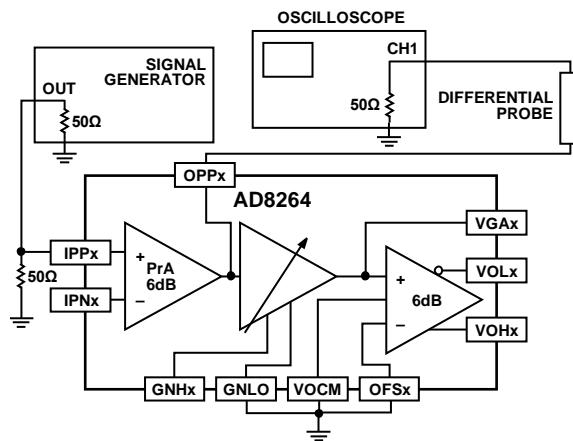


Figure 107. Preamplifier Overdrive Recovery (See Figure 66)

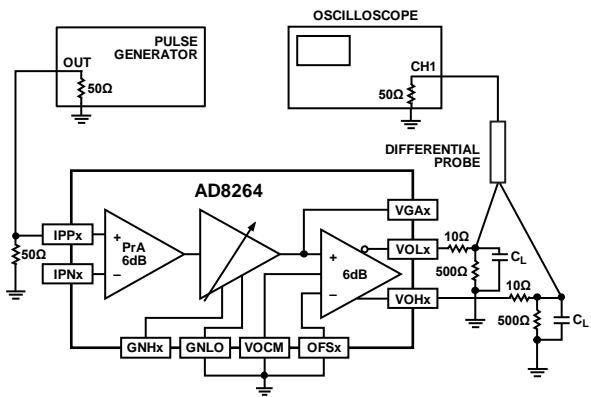


Figure 105. Pulse Response to Differential Output for Various Capacitive Loads with Series $R = 10\ \Omega$, $V_{GAIN} = 0.7$ V (See Figure 63)

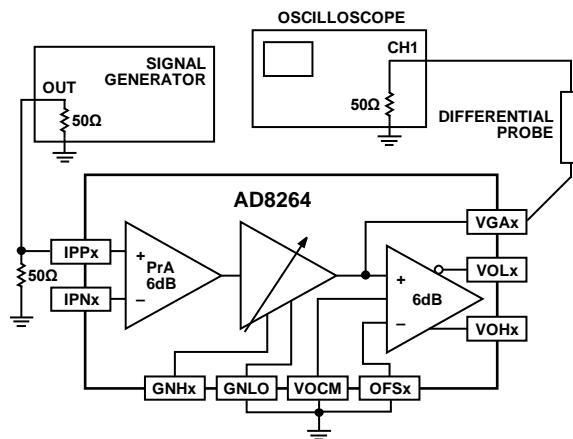


Figure 108. VGA Overdrive Recovery, $V_{GAIN} = 0.7$ V (See Figure 67)

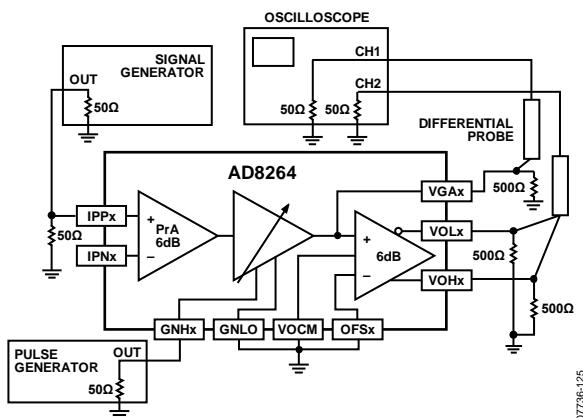


Figure 106. Gain Response to VGAx or Differential Output (See Figure 64 and Figure 65)

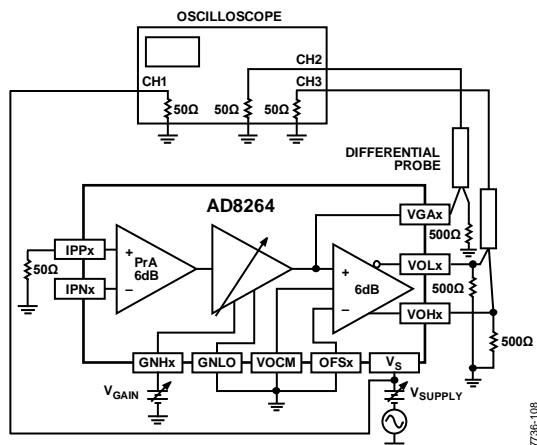


Figure 109. PSRR (See Figure 68 and Figure 69)

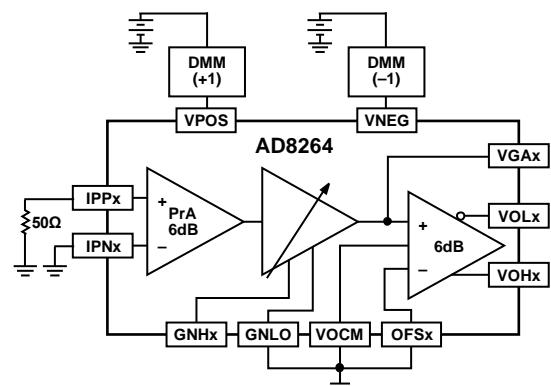


Figure 110. Quiescent Supply Current (See Figure 70)

THEORY OF OPERATION

OVERVIEW

The AD8264 is a dc-coupled quad channel VGA with a fixed gain-of-2 (6 dB) preamplifier and a single-ended-to-differential output amplifier with level shift capability that can be used as an ADC driver. Figure 111 shows a representative block diagram of a single channel; all four channels are identical. The supply can operate from ± 2.5 V to ± 5 V. The primary application is as a pulse processor for medical positron emission tomography (PET) imaging; however, the part is useful for any dc-coupled application that can benefit from variable gain.

The signal chain consists of three fundamental stages: the preamplifier, the variable gain amplifier, and the differential output buffer amplifier. The preamplifier has an internally fixed gain-of-2 (6 dB). The VGA comprises an attenuator that provides 0 dB to 24 dB of attenuation, followed by a fixed gain 18 dB (8x) amplifier. The single-ended VGA output is connected directly to the noninverting input of the differential output (post) amplifier, which has a differential fixed gain-of-2 (6 dB).

The gain range from the preamp input to the VGA output is 0 dB to 24 dB. The aggregate gain range from preamp input to the differential postamplifier output is 6 dB to 30 dB.

The ideal gain equation for the gain from the single-ended input to the output is

$$V_{GAIN} = V_{GNHx} - V_{GNLO} \quad (1)$$

$$Gain = 20 \frac{dB}{V} \times V_{GAIN} + ICPT \quad (2)$$

The ideal value for ICPT, or the intercept, is defined at $V_{GAIN} = 0$ V. The ICPT for the VGA output and differential amplifier outputs equals 12.1 dB and 18.1 dB, respectively. The actual intercept varies with any additional gain or loss along the signal path. The measured values are both approximately 0.2 dB low.

PREAMP

The preamplifier is a current feedback amplifier, designed to drive the internal 100 Ω gain setting resistors and the resistive attenuator, which together result in a nominal load to the preamplifier of about 113 Ω . Normally, the negative preamp input, IPNx, is not connected externally. The positive input IPPx is the high impedance input of the current feedback amp. Note that, at the largest supply voltage of ± 5 V, the input signal can become so large that the preamplifier output cannot deliver the required current to drive the 113 Ω load and, therefore, limits at 6 V p-p. This means that the input limits at 3 V p-p.

The short-circuit input referred noise at maximum VGA gain is about 2.3 nV/ \sqrt{Hz} , and this accounts for all of the amplifiers and gain setting resistors. When measuring the input referred noise from the VGA output, the number is slightly lower at 2.1 nV/ \sqrt{Hz} because the noise of the postamplifier is not included in the noise calculation.

VGA

The VGA has a voltage feedback architecture and uses analog control to vary the gain. Its low gain range helps to maintain low offset and is intended for gain trim applications. The offset of the preamp and the VGA are trimmed; therefore, the maximum input referred offset is <0.5 mV over temperature (see Figure 26). Keeping the gain of each stage relatively low also allows the bandwidth to stay high.

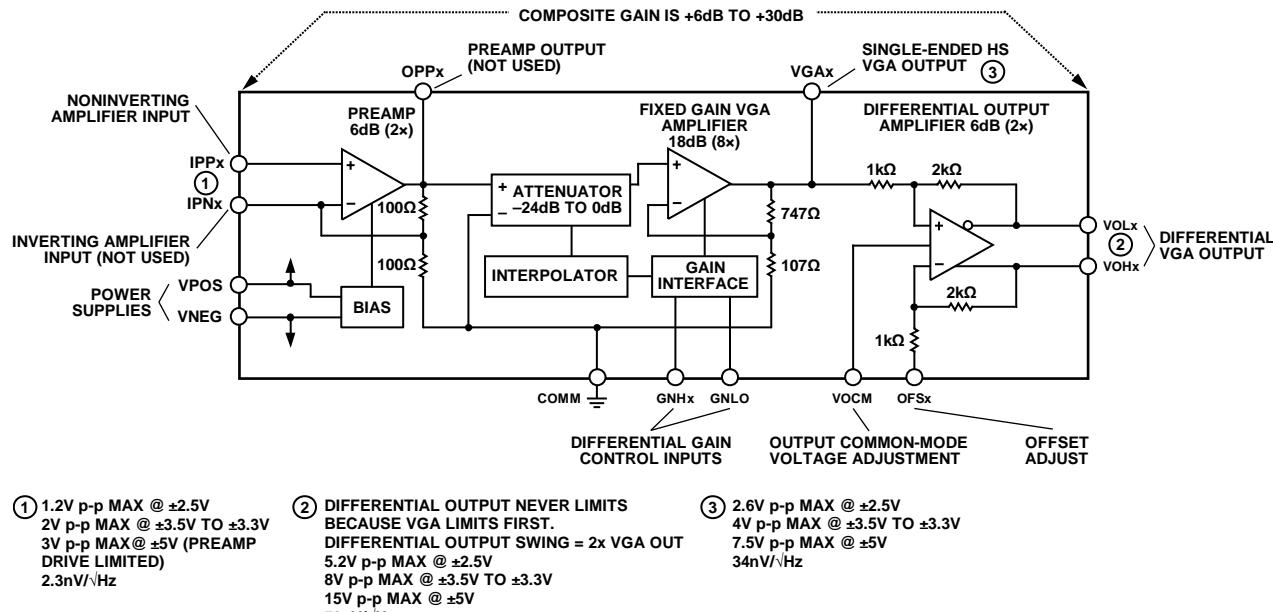
The gain of the VGA is adjusted using the fully differential control inputs, GNHx and GNLO. The GNLO pin is internally connected to all four channels and must be biased externally. Under typical conditions, the GNLO pin is grounded. The gain high control pins (GNHx) are independent for each channel. The gain slope is nominally 20 dB/V. With GNLO connected to ground, each GNHx input can have a voltage applied from VNEG to VPOS without gain foldover.

To make use of the full gain range of the VGA, the nominal gain control voltage needed at GNHx is ± 0.65 V relative to the voltage applied to GNLO. At the lowest supply voltage of ± 2.5 V, the pin GNLO should always be grounded. With increasing supply, the common-mode range of the gain control interface increases. This means that GNLO can be anywhere within ± 1.2 V at ± 3.3 V supplies and ± 2.8 V at ± 5 V supplies.

Table 5. Gain Control Input Range

Supply Voltage (V)	GNLO Voltage Range (V)	V_{GAIN} Range (V)
± 5	± 2.8	± 0.65
± 3.3	± 1.2	± 0.65
± 2.5	0	± 0.65

For example, at ± 3.3 V supplies, the outputs of a single-supply unipolar DAC, such as the 10-bit, 4-channel [AD5314](#), can be used to drive the GNHx pins directly, in conjunction with using the [ADR318](#) 1.8 V reference to bias the GNLO pin at $V_{REF}/2 = 0.9$. Because the GNLO pin sources only about 1.2 μ A for the four channels (~ 300 nA per channel, the same as for the GNHx pins), a simple resistive divider is generally adequate to set the voltage at the GNLO input.



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Figure 111. Single-Channel Block Diagram

POST AMPLIFIER

From the preamp input to the VGA output (VGAx), the gain is noninverting. As can be seen in Figure 111, the VGAx pins drive the positive input of the differential amplifier. The gain is inverting from the input of the preamp to the output pin at VOLx, and the gain is noninverting to the output VOHx.

Other than the input from VGAx, each differential amplifier has two additional inputs: VOCM and OFSx. A common VOCM pin is shared among all four postamplifiers, while separate OFSx pins are provided for each channel.

VOCM Pin

The VOCM pin sets the common-mode voltage of the differential output and must be biased by an external voltage. When driving a dc-coupled ADC, the voltage typically comes from the ADC reference, as shown in the Applications Information section.

If dc level shift is not necessary, the VOCM pin is connected to ground.

OFSx Pins

The OFSx pins are the inverting inputs of the differential post amplifiers and can be used to prebias a differential dc offset at the output. This is very useful when the input is a unipolar pulse because the user can set up the gain and the offset in such a way as to optimally map a unipolar pulse into the full-scale input of an ADC, while dc coupling throughout.

If dc offset is not desired, then the OFSx pins should be connected to ground. However, the OFSx pins can also be used as separate inputs if the user wants this function.

NOISE

At maximum gain, the preamplifier is the primary contributor of noise and results in a differential output referred noise of roughly 73 nV/ \sqrt{Hz} . The noise at the VGAx outputs is 34 nV/ \sqrt{Hz} , and because of the gain-of-2, the VGA output noise is amplified by 6 dB to 68 nV/ \sqrt{Hz} . The differential amplifier, including the gain setting resistors, contributes another 26 nV/ \sqrt{Hz} , and the rms sum results in a total noise of 73 nV/ \sqrt{Hz} . At the lowest gain, the noise at the VGA output is approximately 19 nV/ \sqrt{Hz} , and when multiplied by two, it results in 38 nV/ \sqrt{Hz} at the differential output; again, rms summing this with the 26 nV/ \sqrt{Hz} of the differential amplifier causes the total output referred noise to be approximately 46 nV/ \sqrt{Hz} .

The input referred noise to the preamplifier at maximum gain is 2.3 nV/ \sqrt{Hz} and increases with decreasing gain. Note that all noise numbers include the necessary gain setting resistors.

APPLICATIONS INFORMATION

A LOW CHANNEL COUNT APPLICATION CONCEPT USING A DISCRETE REFERENCE

The AD8264 is particularly well suited for use in the analog front end of medical PET imaging systems. Figure 112 shows how the AD8264 may be used with the [AD5314](#) (a 4-channel, 10-bit DAC) and the [AD9222/AD9228](#) (an octal or quad, 12-bit ADC, respectively). The DAC sets the gain of the AD8264. Note that the full gain span of 24 dB is achieved with this setup because the gain control input range of the AD8264 is very close to 1.25 V. The GNLO pin must offset by $1.25/2 = 625$ mV because the gain control input is bipolar around the voltage applied at GNLO. This is done with two $1\text{ k}\Omega$, 1% resistors. The approximately $1\text{ }\mu\text{A}$ of bias current flowing from the GNLO pin does not contribute a significant error because the basic gain error of the AD8264 is the limiting factor.

The **ADR127** 1.25 V precision reference with an input of 3.3 V can supply -2 mA to $+5 \text{ mA}$ from -40°C to $+125^\circ\text{C}$, which is sufficient to drive both the resistive divider and the **REFIN** pin of the **AD5314**. The **AD5314** is based on the string DAC concept, which means that the **REFIN** pin looks like a resistor that is nominally $45 \text{ k}\Omega$; this results in a current draw of $1.25\text{V}/45 \text{ k}\Omega = 28 \text{ }\mu\text{A}$. Even at the lowest specified resistance of $37 \text{ k}\Omega$, this is still only a current of $34 \text{ }\mu\text{A}$. Therefore, the total current draw from the **ADR127** is the $625 \text{ }\mu\text{A}$ of the resistive divider plus $\sim 30 \text{ }\mu\text{A}$, which equals $\sim 655 \text{ }\mu\text{A}$, well below the 5 mA maximum current.

Figure 112 also includes the DAC output equation, which indicates that the output can vary between 0 V and $V_{REF} = 1.25$ V.

The output of the AD8264 is ideal to drive an ADC like the 1.8 V quad-channel AD9228. If eight channels are needed, two AD8264s with the octal AD9222 ADC achieve the same thing. The same resistive divider can be used for two AD8264s because the bias current flowing is now $\sim 2 \mu\text{A}$, but this still only introduces an error of 1 mV with ideally matched resistors. With 20 dB/V gain scaling, this is a gain error of only 0.02 dB, which is much smaller than the fundamental gain error of the AD8264 (typically $\sim 0.2 \text{ dB}$).

The single-ended-to-differential amplifier of the AD8264 amplifies the VGA output signal by 6 dB and can provide the required dc bias of the AD9222/AD9228, as shown in Figure 112. The ADC is connected with the default internal reference because the SENSE pin is grounded. With this connection, the AD9222/AD9228 VREF pin is an output that provides 1 V; this is then connected to the VOCM input of the AD8264, which sets the output common-mode voltage of the VOHx and VOLx pins to 1 V. This voltage is very close to the recommended optimal value of $VDD/2 = 0.9$ V. With this configuration, the ADC inputs are set to a full-scale (FS) of 2 V p-p.

Note that the ADC VREF should not drive many loads; therefore, for multiple AD8264s, the VREF should be buffered.

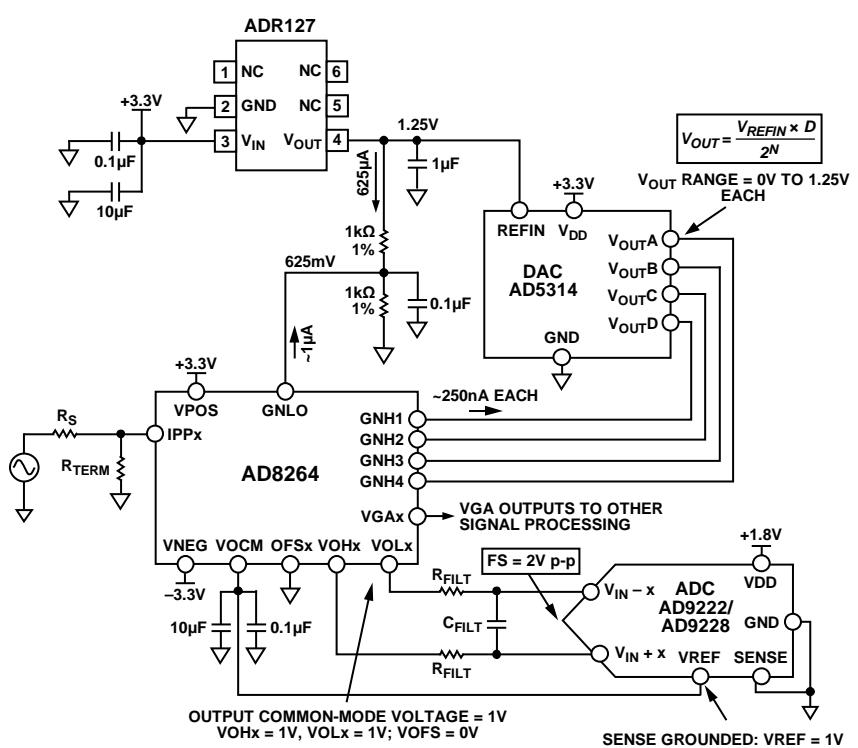


Figure 112. Application Concept of the AD8264 with the AD5314 10-Bit DAC and the AD9222/AD9228 12-Bit ADC

A DC CONNECTED CONCEPT EXAMPLE

The dc connected concept example in Figure 113 is an application with the 40-channel **AD5381**, 3 V, 12-bit DAC. The main difference between this example and Figure 112 is that, for the same **ADR127** 1.25 V reference, the full-scale output of the DAC is from 0 V to $2 \times \text{VREFIN} = 2.5$ V. Two options for gain control include the following:

- Use the same circuit as in Figure 112 but use only half the DAC output voltage from 0 V to 1.25 V. This is the simplest solution, requiring the fewest extra components. Note that the overall gain resolution increases by one bit to 11 bits over the 10-bit **AD5314**.
- Ground GNLO and scale the DAC output so that the GNHx inputs vary from -0.652 V to $+0.625$ V. Figure 113 shows a possible circuit implementation using a divider between the DAC output and a -1.25 V reference.

GNLO cannot simply be increased to 1.25 V because, for a given supply voltage, GNLO has a limited voltage range to achieve the full gain span (see Table 5).

However, a third possibility is to use another voltage that is between 1.2 V and 625 mV on GNLO, such as 1 V. In this case, the DAC must vary from 0.375 V to 1.625 V to achieve the fully specified gain range.

Note the gain limits when the differential gain control exceeds ± 0.625 V, either to 6 dB or to 30 dB. If the differential gain control input voltage is exceeded, no gain foldover occurs.

Figure 113 shows how the AD8264 is connected in a PET application. The PMT generates a negative-going current pulse that results in a voltage pulse at the preamplifier input and a differential output pulse on VOLx and VOHx.

To fully appreciate the advantages of the AD8264, note the common-mode and polarity conversion afforded. The **AD9228**, as with most modern ADCs, is a low voltage, single-polarity device. Recall that the PMT is a high voltage device that yields a negative pulse. To map the pulse to the input range of the ADC, the pulse must be inverted, shifted, and amplified to the full input range of the ADC. This is done by using the gain control, signal offset, and common-mode features of the AD8264.

The full-scale input of the converter is 0 V to 2 V, with a common-mode of 1 V. Match the VOCM voltage of the AD8264 to the ADC common mode (VREF = 1 V), and the two devices can be connected directly using an appropriate level of the antialiasing filter. The PMT signal is 0 V to -0.1 V. With a gain of $20 \times$ (26 dB), the AD8264 output signal range is 2 V p-p. Prebias the signal negative by -0.5 V using the AD8264 OFSx inputs, which sets VOHx = 1.5 V and VOLx = 0.5 V for VOCM = 1 V. The output is perfectly matched to the input of the ADC.

Note that, by connecting VOLx to the positive ADC input and VOHx to the negative ADC input, the negative input pulse is inverted automatically. The VGAx output is still a negative pulse, amplified by 20 dB for this example.

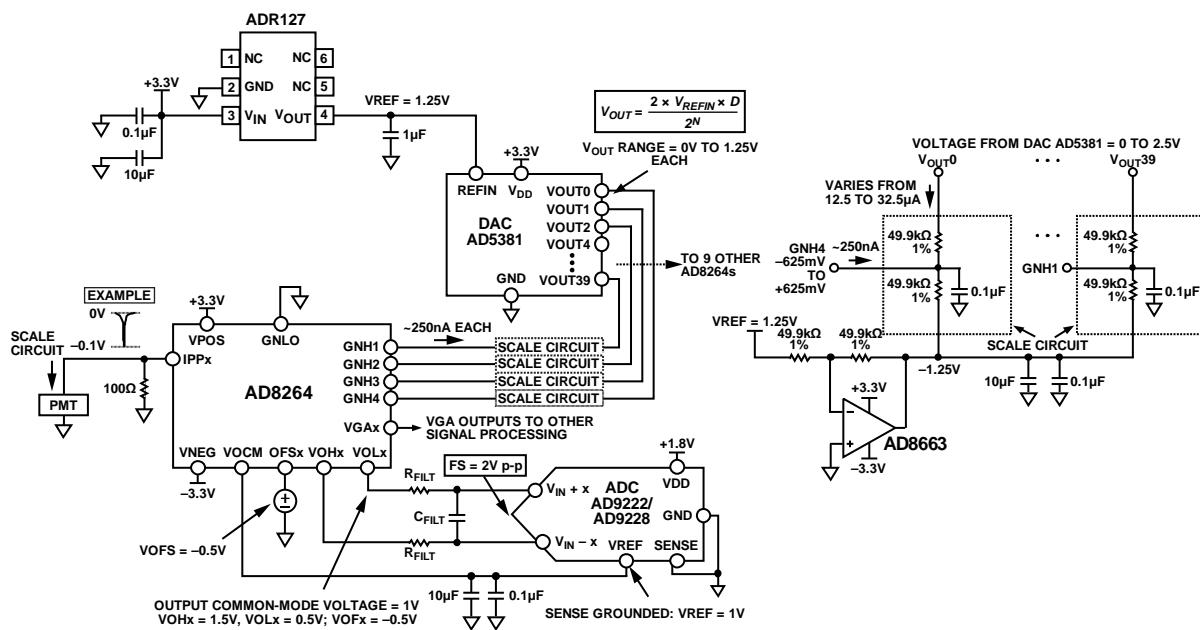


Figure 113. Concept Application of AD8264 with 40-Channel AD5381 12-Bit, 3 V DAC and AD9222/AD9228 12-Bit ADC

AD8264

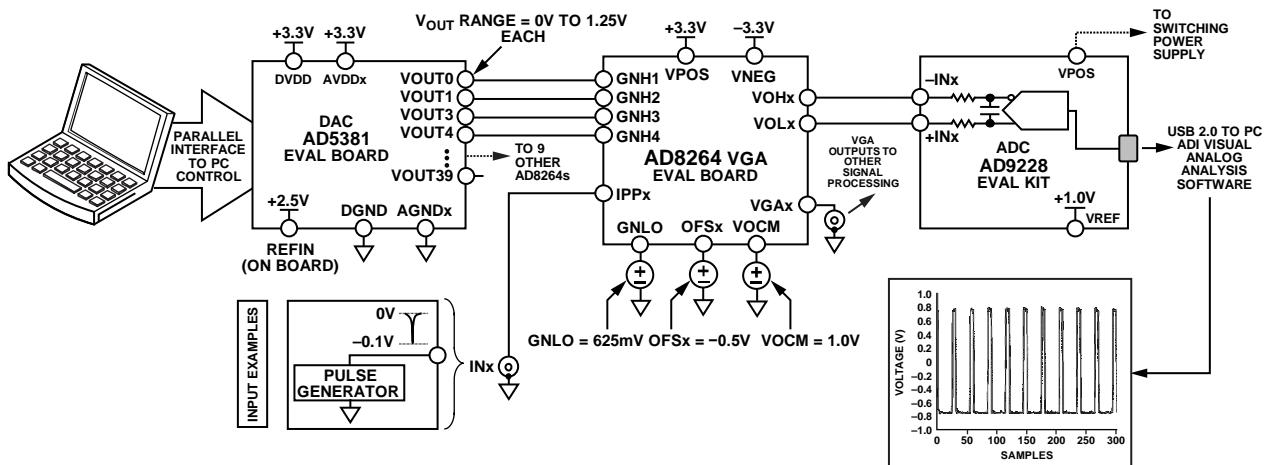


Figure 114. Evaluation Setup for DC-Coupled Analog Front-End Pulse Processing Application Using the AD8264

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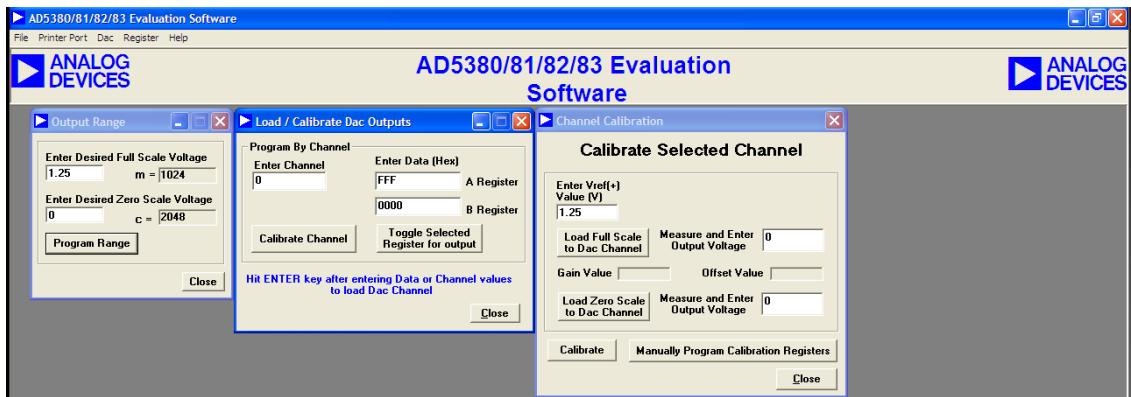


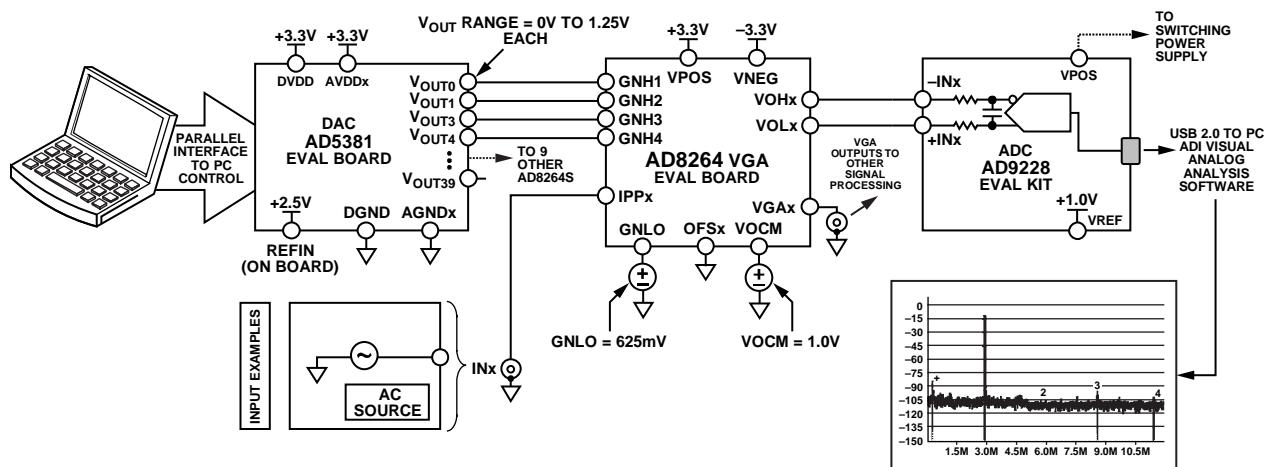
Figure 115. AD5381 Evaluation Software

A convenient method of verifying and customizing the signal chains shown in Figure 112 or Figure 113 is by ordering the corresponding evaluation boards available on www.analog.com. The AD8264-EVALZ is a platform through which the user can quickly become familiar with the features and performance capabilities of the AD8264. See the Evaluation Board section for more information.

The **EVAL-AD5381EB** (40-channel DAC) includes a parallel PC interface and software evaluation program to control the DAC. The AD5381 evaluation software allows the user to configure

and program such DAC parameters as input codes, offset level, and output range based on a 2.5 V or 1.25 V reference. For example, as shown in Figure 114, the reference can be set to 1.25 V, with a 0 V to 1.25 V output range to drive the GNHx inputs.

The ADC evaluation kit includes the [AD9228-65EBZ](#) board and HSC-ADC-FIFO5 board to decode the ADC output. It also leverages the capabilities of VisualAnalog®, powerful simulation and data analysis software that enables the user to run FFTs and to do real-time capture of the output levels.



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EVALUATION BOARD

Analog Devices, Inc. provides evaluation boards to customers as a support service so that the circuit designer can become familiar with the device in the most efficient way possible. The AD8264 evaluation board provides a fast, easy, and convenient means to assess the performance of the AD8264 before going through the hassle and expense of design and layout of a custom board. The board is shipped fully assembled and tested, and it provides basic functionality as shipped. Standard connectors enable the user to attach standard lab test equipment without having to wait for the rest of the design to be completed. Figure 117 shows a digital image of the top view, and Figure 118 shows the schematic diagram of the AD8264 evaluation board.

The printed circuit board (PCB) artwork for all conductor and silk-screen layers is shown in Figure 119 to Figure 124. A description of a typical test setup can be found in the Applications Information section. The PCB artwork can be used as a guide for circuit layout and placement of parts. This is particularly useful for multiple function circuits with many pins, requiring multiple passive components.

CONNECTING AND USING THE AD8264-EVALZ

The AD8264 operates with bipolar power supplies from ± 2.5 V dc to ± 5 V dc. Make sure the current capacity is ≥ 400 mA. Connect a ground reference from the supplies to any of the black test loops, the positive supply to the red test loop (+V), and the negative supply to the blue test loop (-V).

Notice that the board is shipped with jumpers installed on the 2-pin headers marked GN1_2, GN3_4, OFS_12, OFS_34, GNLO, and VOCM. If these jumpers are missing, the offset and common-mode functions float high, substantially increasing the quiescent current of the board.

Apply input signals to any of the preamps at the SMA connectors, IN1 through IN4. These connectors are terminated with $50\ \Omega$ to accommodate typical signal generator analyzer voltage source impedances. The gain of the AD8264 preamps is fixed at 6 dB (2 \times) and can be monitored at the SMA connectors, OP1_2 and OP3_4, if desired. Note that there are output selector switches for each pair of preamps and $453\ \Omega$ resistors in series with the preamp outputs.

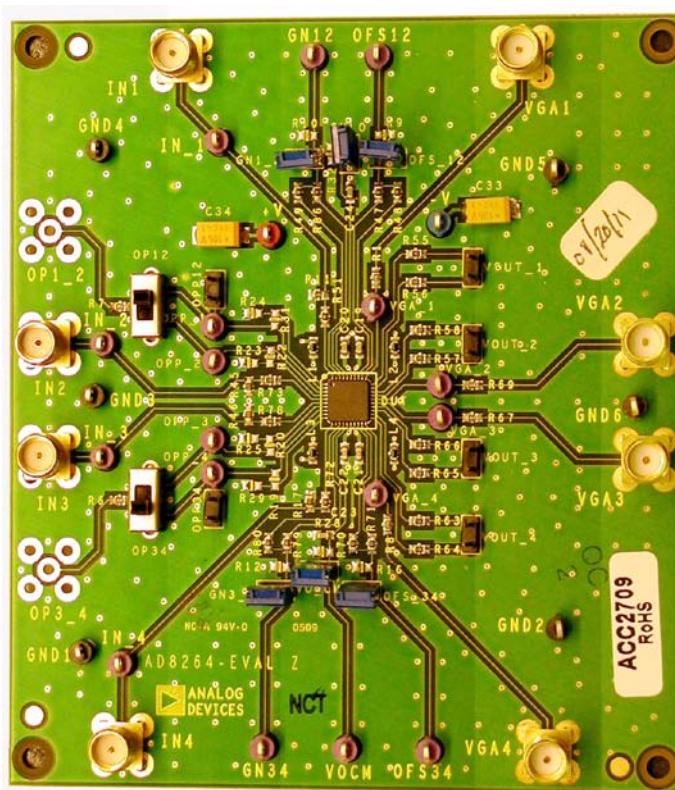


Figure 117. Digital Image of the AD8264-EVALZ (Top View)

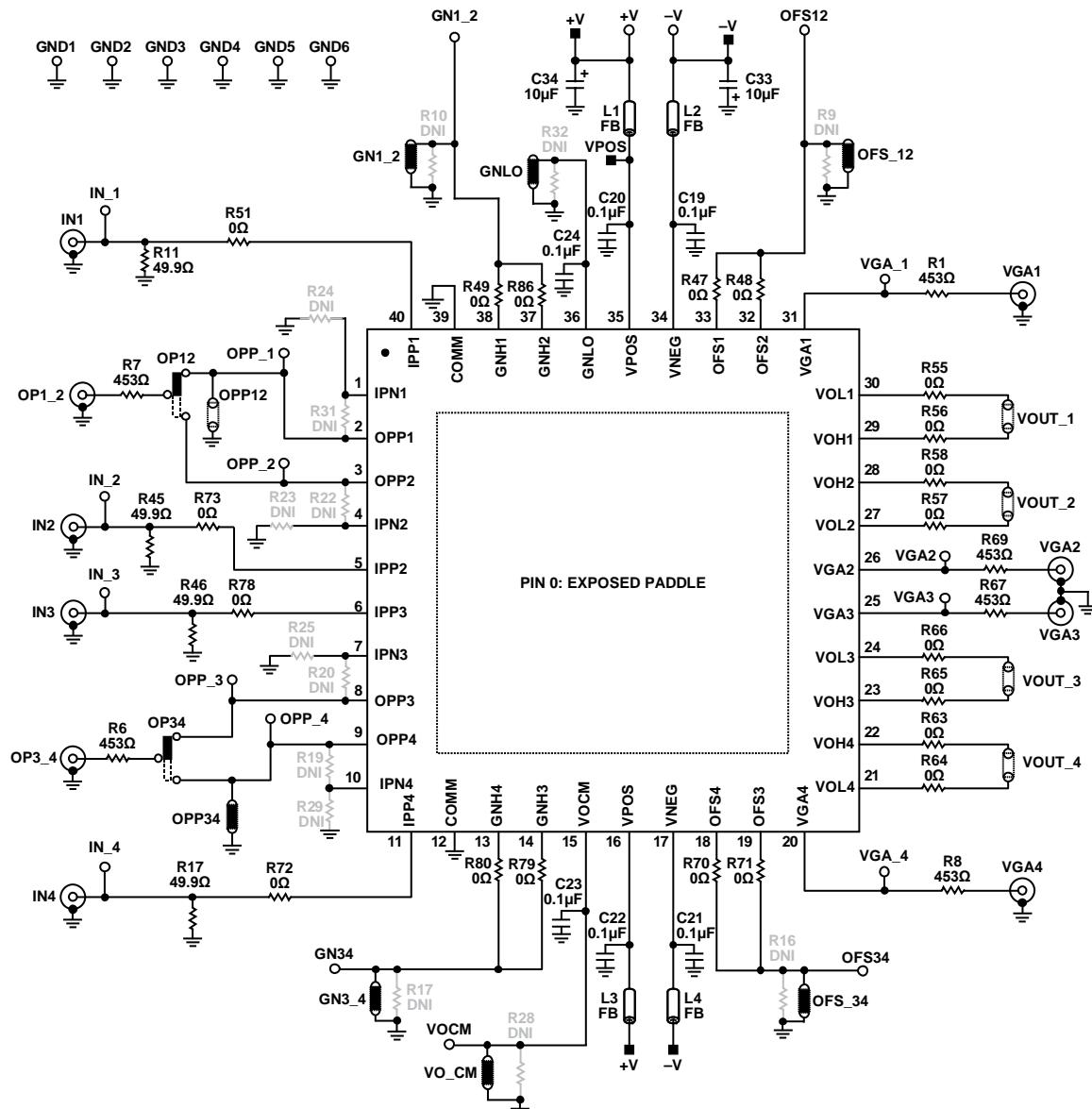


Figure 118. AD8264-EVALZ Schematic

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The SMA connectors, VGA1 through VGA4, enable signal monitoring at these nodes, with $453\ \Omega$ resistors for protecting the device. These resistors can be shorted at the discretion of the user if wide bandwidth is desired. The differential outputs are provided with 0.1" spacing 2-pin headers, which fit the low capacitance Tektronix differential scope probe P6045 model.

Note that the gain control input of the AD8264 is differential. Each channel has its own gain control pin (GNH_x); however, pairs of pins are connected together on the evaluation board and connected to a test loop. The 2-pin headers are provided for jumpers to connect the gain pins to ground, preventing the

quiescent gain control voltage at the GNH_x pins from floating high. The low sides of the gain controls for each channel are internally connected in the AD8264, and a 2-pin header with jumper is provided to connect this pin (GNLO) to ground as well.

A similar arrangement of 2-pin headers is provided for the output offset voltage. As shipped, the offset pins are connected to ground, preventing the pins from floating high.

For connecting to an ADC, remove the jumpers at the OF1_2 and OF3_4 headers and connect the appropriate offset voltage at the test loops, OF12 and OF34. If the VO_{CM} pin is buffered, it can be connected to the reference of the ADC.

AD8264

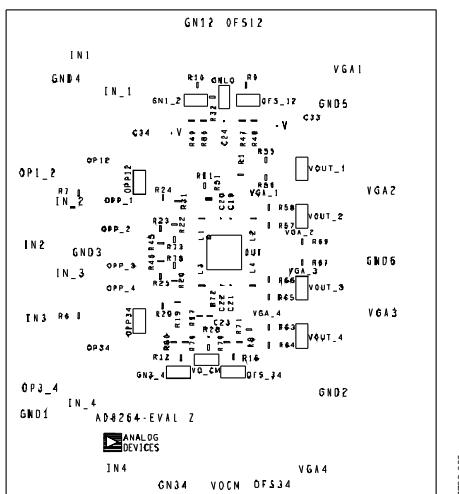


Figure 119. Component Side Assembly

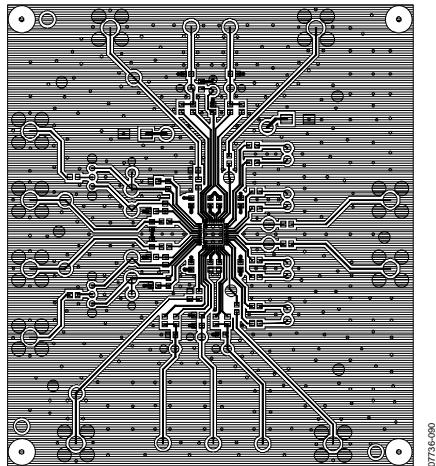


Figure 120. Component Side Copper

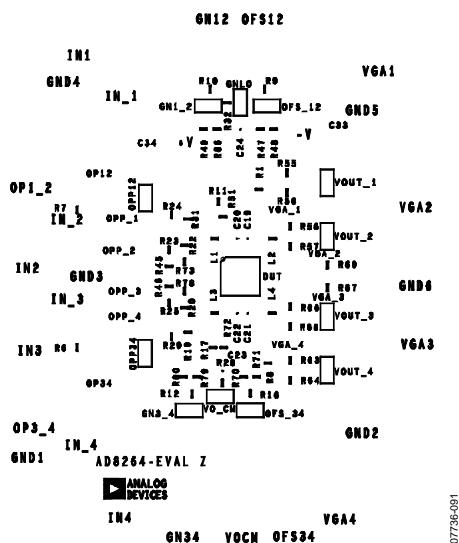


Figure 121. Component Side Silk Screen

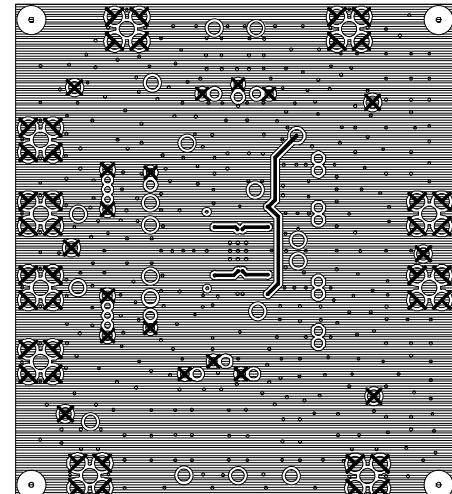


Figure 122. Secondary Side Copper

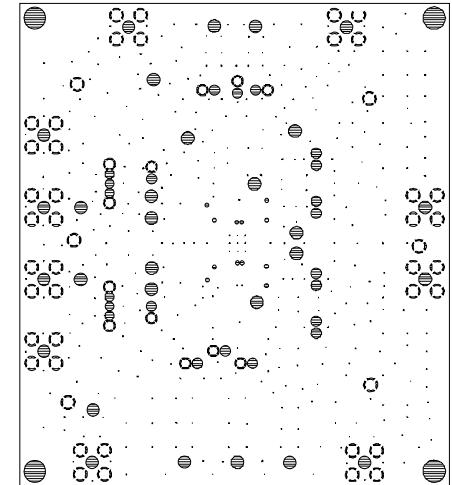


Figure 123. Ground Plane

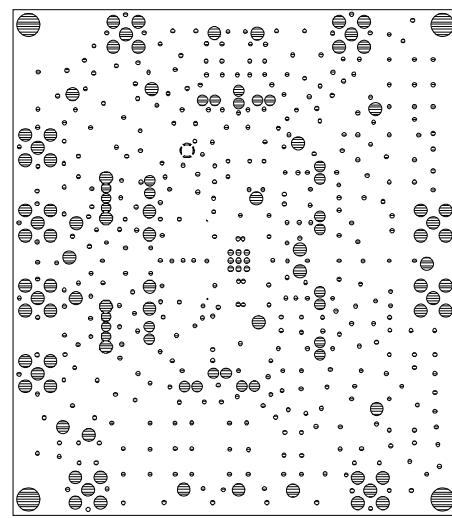


Figure 124. Power Plane

OUTLINE DIMENSIONS

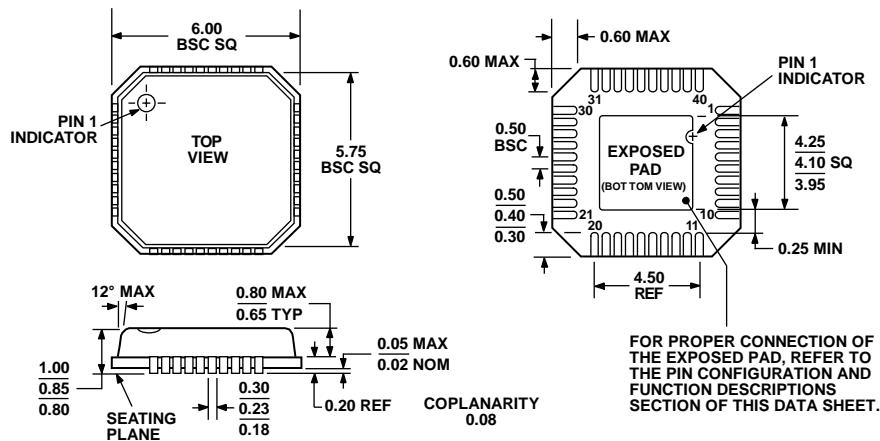


Figure 125. 40-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
6 mm × 6 mm Body, Very Thin Quad
(CP-40-1)
Dimensions shown in millimeters

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ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option	Branding
AD8264ACPZ	–40°C to +85°C	40-Lead LFCSP_VQ	CP-40-1	H1V
AD8264ACPZ-R7	–40°C to +85°C	40-Lead LFCSP_VQ, 7" Tape and Reel	CP-40-1	H1V
AD8264ACPZ-RL	–40°C to +85°C	40-Lead LFCSP_VQ, 13" Tape and Reel	CP-40-1	H1V
AD8264-EVALZ		Evaluation Board		

¹ Z = RoHS Compliant Part.

AD8264

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